1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
C	0000813234	PRODUCTION RELEASED	2009-11-01

K84 MLB SCHEMATIC

PROD OK2FAB 11/01/2009

Page (.csa)		Contents	Sync	Date
1	1	Table of Contents	K24_MLB	01/19/2009
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12	12	CPU Decoupling	K24_MLB	03/30/2009
13	13	eXtended Debug Port(MiniXDP)	K24_MLB	02/25/2009
14	14	MCP CPU Interface	K24_MLB	04/06/2009
15	15	MCP Memory Interface	K24_MLB	04/06/2009
16	16	MCP Memory Misc	K24_MLB	04/06/2009
17	17	MCP PCIe Interfaces	K24_MLB	04/06/2009
18	18	MCP Ethernet & Graphics	K24_MLB	04/06/2009
19	19	MCP PCI & LPC	K24_MLB	04/06/2009
20	20	MCP SATA & USB	K24_MLB	04/06/2009
21	21	MCP HDA & MISC	K24_MLB	03/24/2009
22	22	MCP Power & Ground	K24_MLB	04/06/2009
23	25	MCP Standard Decoupling	K24_MLB	04/06/2009
24	26	MCP Graphics Support	K24_MLB	04/06/2009
25	28	SB Misc	K24_MLB	02/15/2009
26	29	FSB/DDR3 Vref Margining	K24_MLB	04/06/2009
27	31	DDR3 SO-DIMM Connector A	K24_MLB	02/05/2009
28	32	DDR3 SO-DIMM Connector B	K24_MLB	02/05/2009
29	33	DDR3 Support	K24_MLB	04/06/2009
30	34	X16 WIRELESS CONNECTOR	K24_MLB	01/27/2009
31	37	Ethernet PHY (RTL8211CL)	K24_MLB	04/06/2009
32	38	Ethernet & AirPort Support	K24_MLB	04/06/2009
33	39	ETHERNET CONNECTOR	K24_MLB	04/06/2009
34	45	SATA Connectors	K24_MLB	01/19/2009
35	46	External USB Connectors	K24_MLB	02/05/2009
36	49	SMC	K24_MLB	04/02/2009
37	50	SMC Support	K24_MLB	02/04/2009
38	51	LPC+SPI Debug Connector	K24_MLB	02/15/2009
39	52	K84 SMBUS CONNECTIONS	K24_MLB	01/19/2009
40	53	VOLTAGE SENSING	K24_MLB	04/06/2009
41	54	Current Sensing	K24_MLB	01/27/2009
42	55	Thermal Sensors	K24_MLB	02/04/2009
43	56	Fan	K24_MLB	04/06/2009
44	57	WELLSPRING 1	K24_MLB	03/04/2009
45	58	WELLSPRING 2	K24_MLB	02/25/2009
46	59	SMS	K24_MLB	03/04/2009
47	60	DEBUG SENSORS AND ADC	K19_IMLB	02/25/2009
48	61	SPI ROM	K24_MLB	02/15/2009
49	62	AUDIO: CODEC/REGULATOR	AUDIO	06/09/2009
50	63	AUDIO: LINE INPUT FILTER	AUDIO	06/09/2009
51	65	AUDIO: HEADPHONE FILTER	AUDIO	06/09/2009
52	66	AUDIO: SPEAKER AMP	AUDIO	06/09/2009
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54	68	AUDIO: JACK TRANSLATORS	AUDIO	06/09/2009
55	69	DC-In & Battery Connectors	K24_MLB	02/05/2009
56	70	PBUS Supply/Battery Charger	K24_MLB	02/05/2009
57	72	5V/3.3V SUPPLY		
58	73	1.5V/0.75V DDR3 SUPPLY		
59	74	IMVP6 CPU VCore Regulator	K24_MLB	03/03/2009
60	75	MCP CORE REGULATOR	K24_MLB	02/15/2009
61	76	CPU VTT(1.05V) SUPPLY	K24_MLB	02/04/2009
62	77	MISC POWER SUPPLIES	K24_MLB	03/24/2009
63	78	POWER SEQUENCING	K24_MLB	02/15/2009
64	79	POWER FETS	K24_MLB	02/15/2009
65	90	LVDS CONNECTOR	K24_MLB	02/15/2009
66	93	DISPLAYPORT SUPPORT	K24_MLB	04/06/2009
67	94	DisplayPort Connector	K24_MLB	04/06/2009
68	97	LCD Backlight Driver (MC34845)	VEMURI_K19I	02/09/2009
69	98	LCD Backlight Support	K24_MLB	04/06/2009
70	100	CPU/FSB Constraints	K24_MLB	04/06/2009
71	101	Memory Constraints	K24_MLB	04/06/2009
72	102	MCP Constraints 1	K24_MLB	03/30/2009
73	103	MCP Constraints 2	K24_MLB	04/06/2009
74	104	Ethernet Constraints	K24_MLB	04/06/2009
75	106	SMC Constraints	K24_MLB	04/06/2009
76	107	K84 SPECIAL CONSTRAINTS	K24_MLB	01/19/2009
77	109	K84 RULE DEFINITIONS	K24_MLB	01/19/2009

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7982	1	SCHEM,MLB,K84	SCH	CRITICAL	
820-2567	1	PCBF,MLB,K84	PCB	CRITICAL	

DRAWING TITLE: SCHEM,MLB,K84

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DRAWING NUMBER: 051-7982 SIZE: D

REVISION: C.0.0

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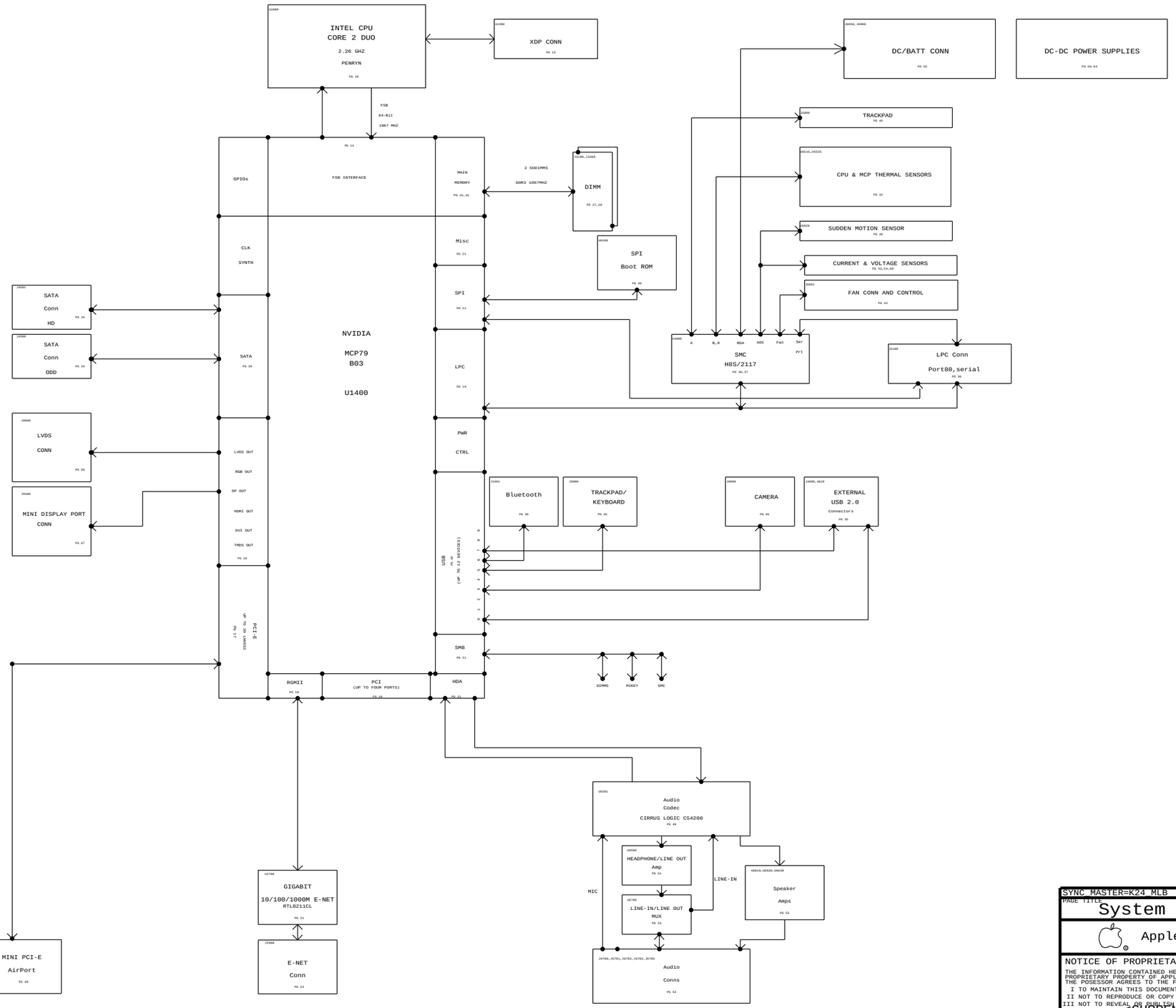

SYNC_MASTER=K24_MLB SYNC_DATE=01/19/2009

PAGE TITLE
System Block Diagram

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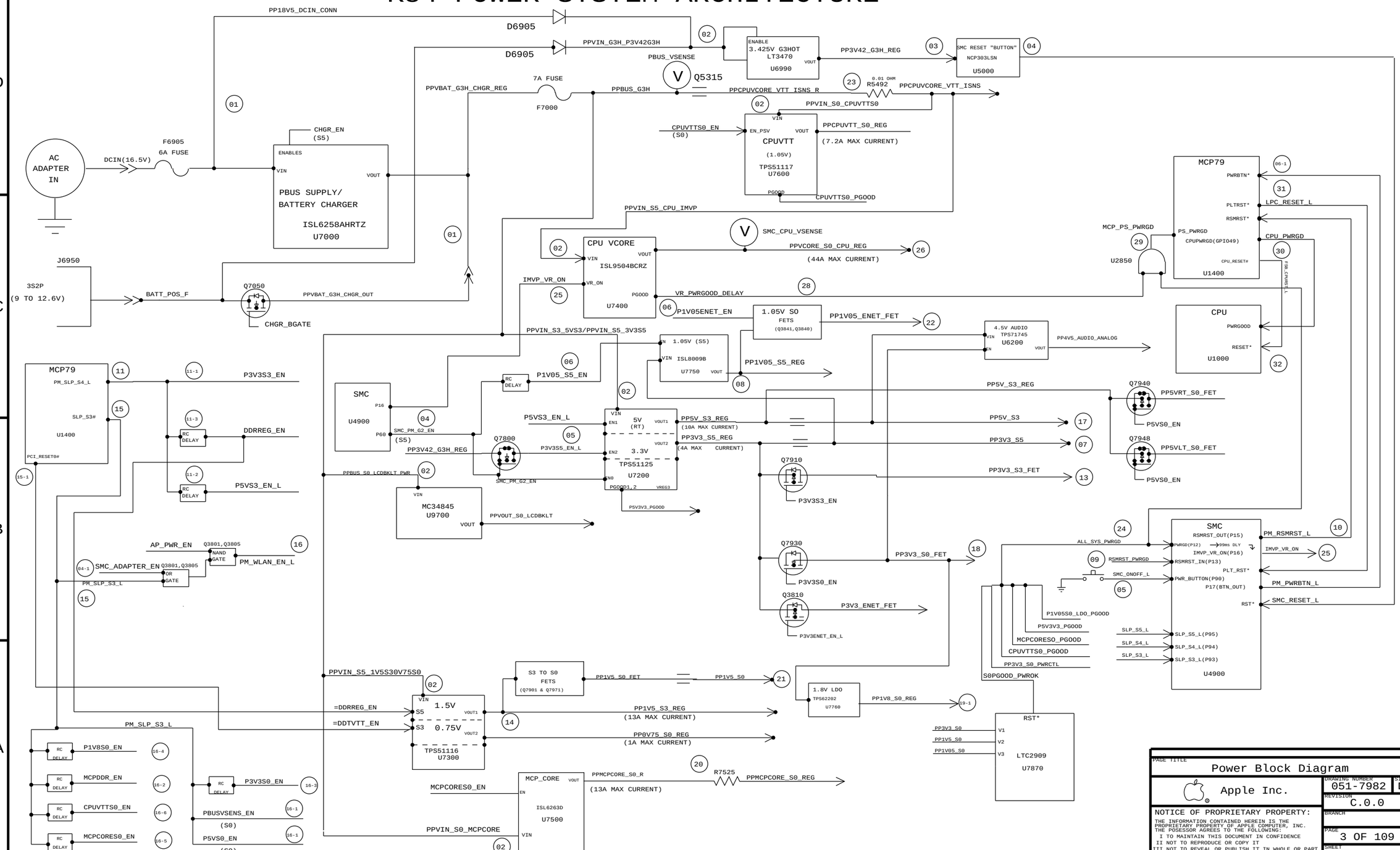
K84 POWER SYSTEM ARCHITECTURE



PAGE TITLE
Power Block Diagram

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0035	PCBA,MLB,FOX DDR CONN,K84	K84_COMMON,CPU_2_0GHZ,FOX_DDR_CONN,EEE_8CG
639-0254	PCBA,MLB,MLX DDR CONN,K84	K84_COMMON,CPU_2_0GHZ,MLX_DDR_CONN,EEE_A36
085-0748	K84 MLB DEVELOPMENT BOM	K84_DEVEL_ENG
639-0554	PCBA,MLB,FOX DDR CONN,PVT K84	K84_COMMON_PVT,CPU_2_0GHZ,FOX_DDR_CONN,EEE_CXR
639-0555	PCBA,MLB,MLX DDR CONN,PVT K84	K84_COMMON_PVT,CPU_2_0GHZ,MLX_DDR_CONN,EEE_CY1
085-1076	K84 MLB DEVELOPMENT PVT	K84_DEVEL_PVT

BOM Groups

BOM GROUP	BOM OPTIONS
K84_COMMON	COMMON,ALTERNATE,K84_MCP,K84_MISC,K84_DEBUG_ENG,K84_PROGPARTS
K84_COMMON_PVT	COMMON,ALTERNATE,K84_MCP,K84_MISC,K84_DEBUG_PROD,K84_PROGPARTS
K84_MCP	MCP_B03,BOOT_MODE_USER,MCPSEQ_SMC
K84_MISC	ONEWIRE_PU,DP_ESD,MIKEY,LDO_NO,MEM_SENSE,1P05_HIGH_SIDE_SENSE,MCP_T_DIODE_SENSOR,MCPSMC_DIGITEMP_YES
K84_PROGPARTS	BOOTROM_PROG,SMC_PROG,WELLSPRING_PROG
K84_DEBUG_ENG	DEVEL_BOM,SMC_DEBUG_YES,XDP
K84_DEBUG_PVT	DEVEL_BOM_PVT,SMC_DEBUG_YES,XDP,NO_VREFMRGN
K84_DEBUG_PROD	SMC_DEBUG_YES,XDP,LPCPLUS_NOT,NO_VREFMRGN
K84_DEVEL_ENG	DEBUG_ADC,XDP_CONN,LPCPLUS,VREFMRGN
K84_DEVEL_PVT	XDP_CONN,LPCPLUS

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3769	1	PDC,SLGVT,2.26,25W,1066,R0,3M,BGA,P7550	U1000	CRITICAL	CPU_2_0GHZ
338S0710	1	IC,GMCP,MCP79,35X35MM,BGA1437,B03	U1400	CRITICAL	MCP_B03
516S0706	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA	J3200	CRITICAL	FOX_DDR_CONN
516-0201	1	CONN,204P,SODIMM,P=0.6MM	J3100	CRITICAL	FOX_DDR_CONN
516S0790	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,NON/SC	J3200	CRITICAL	MLX_DDR_CONN
516-0213	1	CONN,204P,SODIMM,P=0.6MM,HF	J3100	CRITICAL	MLX_DDR_CONN
452-1708	4	SCR.M1.6X0.35X6.0,D4,HO.3,BLK,M97	SCREW1,SCREW2,SCREW3,SCREW4	CRITICAL	
514-0704	1	CONN,RCPT,RJ45,PLASTIC,HF,K83/K84	J3900	CRITICAL	
514-0705	2	CONN,RCPT,USB,4P,PLASTIC,HF,K83/K84	J4600,J4610	CRITICAL	
514-0706	1	CONN,RCPT,MDP,20P,PLASTIC,HF,K83/K84	J9400	CRITICAL	
514-0718	1	CONN,RCPT,S/PDIF,TX,HF,CFR,K83/K84	J6700	CRITICAL	
353S2718	1	IC,ISL88042,4X V MONTR,2.7B/2.86V,TDFN8	U7870	CRITICAL	
870-1885	4	POGO PIN,MED,NOISE-IMPROVED,K84	ZS0900,ZS0901,ZS0902,ZS0903	CRITICAL	
870-1885	3	POGO PIN,MED,NOISE-IMPROVED,K84	ZS0908,ZS0909,ZS0911	CRITICAL	
870-1886	5	POGO PIN,TALL,NOISE-IMPROVED,K84	ZS0904,ZS0905,ZS0906,ZS0907,ZS0910	CRITICAL	
870-1886	5	POGO PIN,TALL,NOISE-IMPROVED,K84	ZS0912,ZS0913,ZS0914,ZS0915,ZS0919	CRITICAL	
870-1887	3	POGO PIN,THIN,NOISE-IMPROVED,K84	ZS0917,ZS0918,ZS0916	CRITICAL	
104S0033	4	RES,MF,1/4W,6.8OHM,5%,0805,SMD	R6612,R6617,R6630,R6633	CRITICAL	
518S0774	1	CONN,RCPT,60P,P=0.4,STK HT 1.0	J1300	CRITICAL	XDP_CONN

353S2718 IS NEW INTERSIL PART FOR FIXING B4 DONGLE ISSUE
514-0704 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0692 PART FOR RJ45 CONNECTOR
514-0705 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0689 PART FOR USB CONNECTORS
514-0706 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0691 PART FOR MINI DP CONNECTOR
514-0718 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0694 PART FOR AUDIO CONNECTOR

DEVELOPMENT BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-0748	1	K84 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
085-1076	1	K84 MLB DEVELOPMENT PVT	DEVEL_PVT	CRITICAL	DEVEL_BOM_PVT

Programmable Parts

338S0563	1	IC,SMC,HS8/2117,9X9MM,TLP,HF	U4900	CRITICAL	SMC_BLANK
341S2485	1	IC,SMC,K84	U4900	CRITICAL	SMC_PROG
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341S2487	1	IC,PRGRM,EFI BOOTROM,UNLOCK,K84	U6100	CRITICAL	BOOTROM_PROG
337S2983	1	IC,PSOC+ W/ USB,56 PIN,MLF,CY8C24794	U5701	CRITICAL	WELLSPRING_BLANK
341S2491	1	IC,WELLSPRING CONTROLLER,K84	U5701	CRITICAL	WELLSPRING_PROG

LOCKED BOOTROM APN IS 341S2488

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0693	152S0778		ALL	DALE/VISHAY, MAGLAYERS AS ALTERNATE
152S0796	152S0685		ALL	CYNTEC AS ALTERNATE
157S0058	157S0055		ALL	DELTA AS ALTERNATE
138S0603	138S0602		ALL	MURATA AS ALTERNATE
128S0093	128S0218		ALL	KEMET AS ALTERNATE
152S0874	152S0516		ALL	MAGLAYERS AS ALTERNATE
152S0847	152S0586		ALL	MAGLAYERS AS ALTERNATE
104S0018	104S0023		ALL	DALE/VISHAY AS ALTERNATE

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:8CG]	CRITICAL	EEE_8CG
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:A36]	CRITICAL	EEE_A36
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:CXR]	CRITICAL	EEE_CXR
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:CY1]	CRITICAL	EEE_CY1

K84 BOARD STACK-UP

Top	SIGNAL
2	GROUND
3	SIGNAL(High Speed)
4	SIGNAL(High Speed)
5	GROUND
6	POWER
7	POWER
8	GROUND
9	SIGNAL(High Speed)
10	SIGNAL(High Speed)
11	GROUND
BOTTOM	SIGNAL

SYNC MASTER=K24 MLB SYNC DATE=01/19/2009

PAGE TITLE
BOM Configuration

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Revision History NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

1/10/2009:INITIAL RELEASE 0.0.1-
- NO CHANGES FROM MLB
- PAGE 33 ADDED 34 REFERENCES WITH K84
- UPDATED SCHEMATIC AND PCB PART NUMBER INFO

1/21/2009: RELEASE 0.0.2-
- DELETED PAGES 41,42,43,48,97,98,105 [FIREWIRE, IR CONTROLLER, BACKLIGHT CKT]
- UPDATED BOM CONFIGURATIONS
- DELETED IR SPECIFIC NETS ON SATA CONNECTOR

1/22/2009: RELEASE 0.0.3-
- CORRECTED BOM CONFIG TABLES

1/21/2009: RELEASE 0.0.4-
- CORRECTED BOM CONFIG TABLE (ADDED BACK BKLT ENG)
- ADDED PAGE PAGES 87-98 (LCD BACKLIGHT DRIVER AND SUPPORT CKT)
- DELETED KB BACKLIGHT DRIVER/DETECTION CKT

1/23/2009: RELEASE 0.0.5- 5V/3.3V & DDR3 POWER SUPPLIES AS PER FLO'S RECOMMENDATIONS
- UPDATED PAGES 73-74 5V/3.3V & DDR3 POWER SUPPLIES AS PER FLO'S RECOMMENDATIONS
- SET SOURCE SYNC OF AUDIO PAGES (52-53, 65-68) FROM LENG'S AUDIO PAGES

1/27/2009: TMLB FIRST RELEASE 0.0.1-
- NAME CHANGED TO TMLB, SO CALLING IT RELEASE 0.0.1
- UPDATED SCHEM AND PCBF PART NUMBER INFO
- UPDATED BOM OPTION TABLE TO REFLECT K84_DEBUG_PROD AND BLANK PROGRAMMED PARTS. ALSO, DELETED BMON_ENG BOM OPTION
- DELETED REMOVED BMON_ENG CIRCUIT
- REMOVED ALL SPECIFIC NETS (PAGE 34 & 52)

2/5/2009: RELEASE 0.0.2-
- CORIED TMLB OVER TO MLB AS K84 WILL BE PENRYN SKU WHILE K83 WILL BE ATOM SKU
- UPDATED THE SCHEMATICS, PCBF AND PCBA PART NUMBERS TWEO
- REPLACED TEXT TMLB WITH MLB THROUGHOUT THE SCHEMATICS
- PAGE 4: UPDATED BOM OPTION TABLE TO REFLECT K84_DEBUG_ENG FOR K84_COMMON BOM GROUP
- PAGE 4: UPDATED DEL_NUMBER - 8CG
- PAGE 4: ADDED 085_DEVELOPMENT BOM_VARIANT & K84_DEVEL_ENG, K84_DEVEL_PVT BOM GROUPS
- PAGE 7: DELETED IR_RX_OUT, PP5V_S3_IR & KBDLED_ANODE, SMC_KBDLED_PRESENT_L
- PAGE 8: DELETED FIREWIRE, IR AND BMON SPECIFIC NETS
- PAGE 8: DELETED R0959_PCIE_EW_PRSNT_L'S PD RESISTOR
- PAGE 9: ADDED UNUSED FIREWIRE, IR, BMON NETS AS TEST POINTS
- PAGE 16: CHANGED ALIAS OF PP_PWE_L TO PP_FW_PWE_L
- PAGE 25: ADDED SMC_KBDLED_PWM ALIAS
- PAGE 55: REPLACED U7200 WITH THERMAL SENSORS U5515 AND U5535 WITH THE CHEAPER VERSION APN 353S2573
- PAGE 72: REPLACE 16V INPUT SIDE CAPS C7280 & C7240 WITH 39UF APN 128S0248 AS PER DAYU'S RECOMMENDATIONS
- PAGE 72: REPLACE U7220 WITH SLI7000T
- PAGE 73: REPLACE 16V INPUT SIDE CAPS C7331 WITH 39UF APN 128S0248 AS PER DAYU'S RECOMMENDATIONS
- PAGE 73: REPLACE U7620 WITH SLI7000T

2/6/2009: MAJOR RELEASE 0.1.0 -
- NO CHANGES SINCE LAST MINOR RELEASE 0.0.2

2/6/2009: WEEKLY RFA BOM RELEASE 0.1.0 -
- NO CHANGES SINCE LAST MAJOR RELEASE 0.1.0

2/15/2009: RELEASE 2.0.0.(WEEKLY RFA)-
- PAGE 3: ADDED TWO ALIASES OF PPBUS (PPBUSA_G3H & PPBUSB_G3H). PPBUSA_G3H FEEDS CORE REGULATORS; CPUVTT, MCP VCORE, CPU VCORE & DDR, WHILE PPBUSB FEEDS 5V/3.3V SUPPLY, LCD BKLT & PPBUS VOLTAGE SENS
- PAGE 3: REPLACED STEREO HEADPHONE JACK WITH NEW PART, ADDED NEW CONNECTOR PART NUMBER, P/N : 132S1059)
- PAGE 33: REPLACED AIRPORT CONNECTOR WITH NEW PART, ADDED NEW CONNECTORS AND UPDATED CONNECTIONS ACCORDINGLY
- PAGE 35: REPLACED SATA HDD CONNECTOR WITH APN 353S0349 AND UPDATED CONNECTIONS ACCORDINGLY
- PAGE 45: REPLACED SATA ODD CONNECTOR WITH APN 353S0350 AND UPDATED CONNECTIONS ACCORDINGLY
- PAGE 47: REPLACED FAN CONNECTOR WITH APN 518S0515) FOR SIL
- PAGE 49: REPLACED ESD DIODES WITH CHEAPER PN 371S0907
- PAGE 50: ADDED PP_TIMER_DEBUG_SENSE TO PP3V3_S3_MCP_VCORE_HIGH SIDE CURRENT SENSE AND MCP MEM VDD CURRENT SENSE CIRCUITS FOR DEVELOPMENT BOM
- PAGE 54: ADDED DEBUG_SENSE BOM OPTION TO THE K84_DEVEL_ENG BOM GROUP
- PAGE 60: REPLACED BATTERY CONNECTOR WITH APN 518S0530 (MAG CONNECTOR
- PAGE 61: ADDED NEW PAGE FOR BBRC LDO REGULATOR, DEVICE PP1V8_S3_BBRC, AS PER THE PAGE NUMBER
- PAGE 72: REPLACE 16V INPUT SIDE CAPS C7288 WITH 39UF OSCON CAP (APN 128S0275) & C7248 WITH 39UF (APN 128S0248)
- PAGE 72: CHANGED C7240 TO 39UF OSCON CAP (APN 128S0248)
- PAGE 72: REPLACED U7220 WITH SLI7000T AND U7240 WITH SLI7000T AND ADDED 10UF MLCC
- PAGE 73: ADDED SENSE RESISTOR R7350 ON 1.5V DDR3 SUPPLY RAIL
- PAGE 77: REMOVED 1.05V S0 PSL LDO CIRCUIT, AND REMOVED LDO_NO_BOM OPTION FROM R7745
- PAGE 75: CHANGED C7571 & C7560 TO 68UF OSCON CAPS (APN 128S0225)
- PAGE 76: REMOVED PSV_L13_EN, PSV_L13_EN_DET POWER SUPPLY ENABLE) AND ADDED R7814, C7814 S3 ENABLE CIRCUIT FOR GENERATING PSVL13S_EN ENABLE FROM PP_L1 POWER SUPPLY
- PAGE 77: ADDED PSV_L13_PGOOD POWER GOOD SIGNAL (WIRED AND WITH OTHER S0 RAILS PGOOD) CORRESPONDING TO 5V LT POWER SUPPLY
- PAGE 78: ADDED 0 OHM ISOLATION RESISTORS ON POWER GOOD SIGNALS (BEFORE WIRED AND)
- PAGE 79: ADDED 5V S0 SELECTOR UPDATED NET NAMES FOR BOTH RECEIVING CIRCUITS ACCORDINGLY
- PAGE 80: UPDATED LVDS CONNECTOR CIRCUIT AS PER STEVE'S RECOMMENDATION. ADDED TERESA SIGNALS
- PAGE 97: ADDED BOM OPTION NOSTUFF TO R9702 AS PER K191
- PAGE 7: REPLACED R9425 WITH 10K PU TO PP1V05_S0_MCP_PLL_UF
- PAGE 8: DELETED PP1V5_S0_BKL, RENAMED PP1V5_S3_BKL_R TO PP1V05_S0_MCP_PLL_UF
- PAGE 8: DELETED PP1V5_S0_MCP_PLL_VLDO, PP3V3_S0_BKL_VDDIO, PP3V3_S0_MCP_PLL_VLDO
- PAGE 8: RENAMED PPVTT_S0_1VS3_PP1V05_S3 TO PPVIN_S5_1V5S3@V75S0
- PAGE 28: DELETED FW_RESET_SIGNAL
- PAGE 28: DELETED KB_BKLT_CIRCUIT
- PAGE 66: UPDATED WLAN DIVIDER CIRCUIT WITH 3V3 POWER RAIL TWSIEAR OF EV
- PAGE 67: ADDED 1.05V POWER SUPPLY WITH CORRECT NET NAMES REFLECTING 1.5V/0.75V INSTEAD OF 1.8V/0.9V AND 4N SYNC WITH PAGE 8 ALIASES
- PAGE 41: REMOVED 152S0778 ALTERNATE PART ENTRY FROM THE ALTERNATE PARTS TABLE SINCE L7260 AS HAS BEEN REPLACED WITH THIS PART
- PAGE 4: REMOVED 104S0018 ALTERNATE PART ENTRY FROM THE ALTERNATE PARTS TABLE

PAGES SYNCED FROM K24 SINCE LAST RELEASE 2.0.0
- PG 50: SWAPPED THE PART NUMBER AND THE ALTERNATE PART NUMBER FOR VR5020. MADE ISL60002 THE ALTERNATE PART

PAGES SYNCED FROM LENG OOI'S AUDIO MLB SINCE LAST RELEASE 2.0.0
- CHANGED SPEAKER AMPS TO LM48310, PLACEHOLDERS FOR LM48311. LM48311 IS THE CSP VERSION OF THE LM48310.
- ADDED LDO FOR LEDS
- REMOVED OPTIONAL STUFFING RESISTORS AROUND THE RE-TASKING JACK ANALOG SWITCH.

2/28/2009: RELEASE 4.0 (RFA RELEASE):
- PAGE 41: ADDED LDO_NO_BOM OPTION
- PAGE 8: RENAMED PP1V05_S0_MCP_PLL_BCK TO__ PP1V05_S0_MCP_PLL_UF_R
- PAGE 8: RENAMED PP3V3_S0_MCP_PLL_VLDO TO PP3V3_S0_MCP_PLL_VLDO
- PAGE 33: ADDED EDGE_TOP CONNECTOR WITH APN 518S0825
- PAGE 34: ADDED EDGE_TOP CONNECTOR WITH APN 518S0825 AND RIGHT CLUTCH CONNECTOR PAGE
- PAGE 34: ADDED NOTE WITH REFERENCE TO 10MS RELAY REQUIREMENT BETWEEN 3.3 WLAN POWER GETTING STABLE AND AIRPORT CARD COMING OUT OF RESET
- PAGE 34: REMOVED NOTE ON AMON AND BMON
- PAGE 67: REPLACED KEYBOARD CONNECTOR WITH APN 518S0738
- PAGE 77: ADDED BACK 1.05V LDO CIRCUIT
- PAGE 90: REPRESHED THE SYMBOL OF U0600, PART NUMBER CHANGED TO 353S2603

3/4/2009: RELEASE 5.0.0 (RFA)-
- PAGE 34: ADDED A TEXT NOTE THAT J3401 (AIRPORT CONNECTOR) COULD CHANGE TO 1.8MM HEIGHT APN 516S0582
- PAGE 34: REPLACED KEYBOARD CONNECTOR WITH THAT OF K24 (APN 518S0837) - SYNC'ED FROM K24
- PAGE 34: REPLACED BATTERY CONNECTOR WITH THAT OF K24 (APN 518S0837)
- PAGE 60: DELETED NOTE REGARDING INDUCTOR FILTER REQUIREMENT ON BATT_POS_F (AS PER JOHN SCHEN)
- PAGE 69: CHANGED U7050 TO 376S0761 AS PER DAYU & K24 DESIGN
- PAGE 70: CHANGED U7080 AND U7001 CHEAPER TO 376S0867 (MAT1128) AS PER DAYU'S RECOMMENDATION
- PAGE 71: DISCONNECTING EN_PSV (PIN 54) FROM PSVLTS3_EN SIGNAL AND CONNECTING IT TO PPSVLT_S3_VSIN (SVR1_PS)
- PAGE 72: L7228 CHANGED TO 152S0778 FOR COST SAVING AS PER DAYU
- PAGE 73: ADDED ONE MORE OSCON 39UF CAP ON INPUT SIDE
- PAGE 73: MOVED THE SENSE RESISTOR NEXT TO INDUCTOR
- PAGE 74: REMOVED UNUSED NETWORK ON U7400 PIN 5 AND PIN 6 AS PER DAYU [R7406, C7410, R7427, R7426]
- PAGE 74: STUFF R7413 AS PER DAYU
- PAGE 74: CHANGED U7400 AND U7402 TO 376S0772 AS PER DAYU
- PAGE 74: CHANGED U7401 AND U7403 TO 376S0772 AS PER DAYU
- PAGE 75: CHANGED R7525 TO 187S0132 FOR COST SAVING AS PER DAYU
- PAGE 76: DELETING PSVL13S_EN_DET AS IT IS NO LONGER NEEDED (SEE ABOVE). ALSO UPDATED ASSOCIATED TEXT NOTE
- PAGE 97: FIXED CONNECTION POINT [DOT] FOR LCDBKLT_VIN
- PAGE 97: ADDED OHMS SERIES RESISTOR ON LCD BKLT PWM FOR DEBUGGING PURPOSES
- PAGE 97: RENAMED LCD_BKLT_PWM TO LVDS_IB_BKL_PWM
- PAGE 97: CHANGED VOPP VALUE TO 8.9V AS PER FREESCALE FEEDBACK
- PAGE 97: ADDED R9720 (22K) AND SWAPPED C9705 AND R9705 LOCATIONS FOR NOISE REDUCTION AS PER FREESCALE RECOMMENDATION
- PAGE 97: ADDED PLACEMENT NOTE ATTRIBUTE TO C9713 AND C9710 FOR PLACING THOSE NEAR L9710

3/20/2009: RELEASE 7.1.0 (MAJOR)-
- PAGE 31 & 32: PIN SWAPS ON THE DDR3 CONNECTOR PAGES FOR ROUTING PURPOSES (REFER TO RON'S EMAIL)

PAGES SYNCED FROM CASEY HARDY'S AUDIO_MLB SINCE LAST RELEASE 7.0.0
- PG: 67, DELETED R6726
- PG: 66, CHANGED C6610/11/30/31 TO 0.015UF
- PG: 68, ADDED R6873
- PG: 68, CORRECTED CODEC OUTPUT SIGNALS TABLE COMMENTS

3/24/2009: RELEASE 7.2.0 (MAJOR)-
- PAGE 4: CHANGE THE CPU TO NEW APNB 337S3704
- PAGE 8: DELETED PPBUS_G3H AS NO NEED FOR THE TWO PPBUS BRANCHES
- PAGE 8: COMBINED TWO SEPARATE PPBUS2B BRANCHES INTO ONE =PPBUS_G3H
- PAGE 9: ADD LVDS_BKLT_EN TO R98_NETLABEL
- PAGE 34: CHANGED J3401 ROUTING CONNECTIONS AS PER NEW PIN OUT DESCRIPTION FROM DIANA
- PAGE 45: MIRROR ED J4500 AND RECONNECTED PINS AS PER NEW PIN OUT DESCRIPTION FROM DIANA
- PAGE 45: CHANGED J4501 ROUTING CONNECTIONS AS PER NEW PIN OUT DESCRIPTION FROM DIANA
- PAGE 59: DELETED SMC_PROSA_SENSE ALIAS AND STUFFED R5805
- PAGE 59: DELETED U5470 INA210 CIRCUIT AS THERE IS NO NEED
- PAGE 74: REMOVED R7660 SENSE RESISTOR AND RENAMED =PPBUS_G3H AS NO NEED TO HAVE TWO PPBUS BRANCHES
- PAGE 79: DELETED R7850 CONNECTION BETWEEN CHGR_AGATE AND CHGR_LOWCURRENT_GATE AS PER DAYU
- PAGE 70: ADDED R7050 (6259_YES) CONNECTION FROM PIN 4 (VREF) TO PM_SLP_S3_L AS PER DAYU
- PAGE 70: AS PER DAYU, ADDED:
  R7051 (6259_YES)CONNECTION BETWEEN CHGR_PIN26 AND CHGR_LOWCURRENT_GATE;
  R7052 (6259_ND)CONNECTION BETWEEN CHGR_PIN28 AND GND_CHGR_SGND;
  R7053 (6259_YES)CONNECTION BETWEEN CHGR_PIN6 AND PP1V8_S3 (VMBY);
  R7054 (6259_ND) CONNECTION BETWEEN CHGR_PIN6 AND GND_CHGR_SGND
- PAGE 73: RENAMED PP5V_S3_REG TO PP5V_S3_REG NET TO VOLTAGE=1.5V
- PAGE 97: STUFF R9716 AS PER KIRAN'S FEEDBACK

3/6/2009: RELEASE 6.0.0 (RFA:)-
- PAGE 4: ADDED 152S0693 AS ALT FOR 152S0778 FOR SUPPLY REDUNDANCY
- PAGE 4: ADDED 138S0066 AS ALT FOR 138S0689 FOR SUPPLY REDUNDANCY
- PAGE 4: ADDED PVR1&4 ALTERNATES FOR 107S0074 --> 107S0130 (R7420) AND 107S0075 (R7200) --> 107S0130
- PAGE 4: ADDED VALEX/VISHAY ALTERNATES FOR 104S0023 --> 104S0018
- PAGE 4: ADDED BOM OPTION 6259_NO TO THE TABLE UNDER K84_MISC_BOM GROUP
- PAGE 7: REPLACED R5240 WITH 10K PU TO PP1V05_S0_MCP_PLL_UF AS BIL IS NO LONGER A POR
- PAGE 8: DELETED =PP3V42_G3H AUDIO AS IT IS NO LONGER USED
- PAGE 8: DELETED =PP3V42_G3H_TPAD ON 91 PIN, BECAUSE THERE IS NO KEYBOARD BACKLIGHT DRIVER
- PAGE 8: DELETED =PP3V42_G3H_5V3V3 EN AS IT IS NO LONGER USED
- PAGE 8: ADDED 3 ADDITIONAL TALL POGO PINS AS PER NEW MCO AND DELETED 2S9009 SHORT POGO AS IT WAS EXTRA
- PAGE 9: ADDED TP ALIASES TO TMVPG, TR_TI_AND_TMVDG_MT
- PAGE 9: ADDED TP ALIASES TO 1V8_S3_AND_1V8_S3_MT POWER RAILS AS PER JOHN SCHEN'S FEEDBACK
- PAGE 34: REPLACED THE AIRPORT CONNECTOR WITH 1.8 MM HEIGHT CONNECTOR APN 516S0582
- PAGE 34: ADDED A TEXT NOTE REFERENCING THE ALTERNATE PART APN 514-0668 (SYNC'ED WITH K24)
- PAGE 40: RENAMED =PP5V_S0_HDD_R TO =PP5V_S0_HDD_P AS PER UNALISED LIST REPORT)
- PAGE 40: ADDED INPUT NET ALIAS FOR SMC_BIL_BUTTON_L (SC_SMC_BIL_BUTTON_L)
- PAGE 57: DELETED TERM_BIL_EBOM, SMC_BATTERY & BIL CONNECTIONS
- PAGE 57: ADDED 2 PCS OF 10K PU RESISTORS, R5762 & R5761 AS PER JOHN SCHEN'S FEEDBACK
- PAGE 59: REPLACED SMS PART WITH THE NEW BOSCH BMA141 ANALOG PART. ADDED R5921 10K PU RESISTOR ON
- PAGE 59: ADDED PP3V3_S0_TPAD ON 91 PIN, REPLACED C5923 WITH 0.01UF CAP AS PER DATA SHEET. AND, REPLACED C5922 CAPACITOR SOLUTION IS BEING USED, PART C3_WLAN IS DELETED BY 6P3V3_S3_WLAN (GOING TO 0235S0)- ALSO, REPLACED PP5V_WLAN WITH PP3V3_WLAN ON PAGE 9 (FUNCTIONAL TESTS POINTS)
- PAGE 34: 6235S0 IS MODIFIED TO 110K RESISTOR. R3454 IS NOSTUFF AND R3453 PULLED UP TO PP3V3_WLAN_F. THIS CHANGE WILL ENSURE 3.3V LEVELS AND PROVIDE MAIN 100MS DELAY SPEC BETWEEN 3.3V POWER RAILS THE CARD GETTING STABLE AND AIRPORT GETTING OUT OF RESET
- PAGE 34: DISCONNECTED PP5V_S3_BT FROM THE CONNECTOR AND REPLACED IT WITH PP3V3_S3_BT (SIMILAR TO M06 CAMERA SIGNALS ARE ROUTED VIA LVDS CONNECTOR. MOVED PP5V_S3 CAMERA POWER CIRCUIT ALONG WITH THE USB CAMERA SIGNALS TO LVDS PAGE. ALSO, RENAMED THIS POWER RAIL TO PP5V_S3_CAMERA ON LVDS PAGE
- PAGE 34: ADDED SENSE RESISTOR R3452 ON PP3V3_WLAN_SIGNAL
- PAGE 34: ADDED CHOKES ON LINE 1 TO 82 SIGNALS. UPDATED PAGE 6 (FUNCTIONAL TEST POINTS) ACCORDINGLY
- PAGE 34: REPLACED L3404 WLAN INDUCTOR WITH LOW DCR 0603 PART. PN 0235S0307
- PAGE 39: REPLACED ETHERNET CONNECTOR WITH APN 514-0668 (SIMILAR TO K36B)

3/25/2009: RELEASE 7.3.0 (MAJOR)-
- DELETED DPC_PA 12V/5V LT POWER SUPPLY) AS THERE IS NO NEED OF A SEPARATE 5V S3/S0 SUPPLY
- PAGE 7: RENAMED PP5V_S3 TO PP5V_S3_REG (FILT' AT PRESENT TO BE CLEANED UP)
- PAGE 8: COMBINED 5V S3 LT AND RT ALIASES INTO ONE =PP5V_S3_REG AND RENAMED NETS (LT & RT NOMENCLATURE CLEAN UP)
- PAGE 8: DELETED =PPVIN_S3_5VLT3Q, =PP5VLT_S3_VSIN NETS
- PAGE 21: ADDED ALIAS MCP_GPIO_A_4 FOR SMLEXT MIC LOAD COMPARATOR CIRCUIT
- PAGE 24: UNSTUFFED R9143 PU ON MCP GPIO_A_4 AS THERE IS ALREADY A 100K PU ON AUDIO PAGE
- PAGE 26: ADDED APN TEXT NOTE FOR SIL CONNECTOR
- PAGE 55: ADDED BC846BM NPN TRANSISTOR (APN 372S0129) TO MCP T-DIODE SENSOR CIRCUIT INSTEAD OF THAN IN CPU T-DIODE SENSOR AND STUFFED C5540
- PAGE 72: RENAMED NETS AND NOTES TO REMOVE REFERENCES TO RT POWER SUPPLY
- PAGE 72: REPLACED R7269 WITH APN 152S0212 AS PER DAYU
- PAGE 72: ADDED C7282 APN 128S0218 IN PARALLEL WITH C7280 AS PER DAYU
- PAGE 73: REPLACED U7320 AND U7321 WITH CSD5885A APN 376S0790 MOSFETS AS PER DAYU
- PAGE 73: REPLACED U7333 AND U7331 WITH 0-9010B-CAPS APN 128S0192
- PAGE 73: ADDED C7274 & C7275 AS PER DAYU & 0.22UF APN 132S0132 CAP TO INCREASE THE SLEW RATE
- PAGE 75: ADDED A NOTE OCP=14 SA TO R7572
- PAGE 75: REPLACED U7560 AND U7561 WITH CSD5885B APN 376S0790 MOSFETS AS PER DAYU
- PAGE 76: CORRECTED MAX OUTPUT NOTE TO REFLECT 2A INSTEAD OF 8A
- PAGE 76: REPLACED U7620 WITH 2 CSD5885B APN 376S0790 MOSFETS AS PER DAYU
- PAGE 77: ADDED P1V05S0_LDO_PGOOD POWER GOOD SIGNAL VIA A 0 OHM RESISTOR TO PIN 3 (PG) OF THE LDO
- PAGE 78: DELETED PSV_L13_PGOOD AS THERE IS NO 5V LT POWER SUPPLY ANYMORE
- PAGE 78: RENAMED PSVRTS3_EN TO PSV5S_EN
- PAGE 78: ROUTED P1V05S0_LDO_PGOOD POWER GOOD SIGNAL TO THE WIRED AND CIRCUIT

3/26/2009: RELEASE 7.4.0 (MAJOR)-
- PAGE 60: REPLACED DUAL PACKAGE OPA330 OPAMPS WITH SINGLE PACKAGE ONES - APN 353S2179 (U0930, U0931, U0940, U0941 - ALSO, ADDED C0931 & C0941
- PAGE 9: DELETED EXTRA HOLE DRILLED FOR PIN 2S0912 AND SCREW HOLES Z0908, Z0909

3/26/2009: RELEASE 7.5.0 (MAJOR)-
- PAGE 73: ADDED SHORT XW7304 FROM PIN 1 OF C7300 TO POWER GND (PIN 18)
- PAGE 72: REPLACED C7282 WITH OSCON APN 128S0248 IN PARALLEL WITH C7280 AS PER DAYU

3/26/2009: RELEASE 7.6.0 (MAJOR)-
- ADDED PLACEMENT NOTES TO XW SHORTS AS PER DAYU
- ADDED DIDT=TRUE ATTRIBUTE TO BOOT/VSETSIGNALS OF ALL THE SWITCHING SUPPLIES
- PAGE 8: DELETED =PP5V_S3_BT AS THERE IS NO BBEDI CONNECTOR
- PAGE 8: ADDED =PP5V_S3_HALL FOR THE EFIELD CONNECTOR
- PAGE 8: ADDED =PP3V3_S3_AUDIO AS NET FOR EFIELD NEW CHANGES BELOW
- PAGE 8: DELETED =PP3V42_G3H_EPROBE&=PP5V_S3_EPROBE&=PPBUS_EPROBE AS THERE HAS BEEN REMOVED
- PAGE 8: ADDED =PP5V_S3_BYPASSFET AS THE 5V S3 BYPASS FET CIRCUIT GOES TO 5V LT S0 FET CIRCUIT
- PAGE 8: ADDED PLACEMENT NOTE TO 0ES
- PAGE 8: ADDED OHM ATTRIBUTE TO THE LVDS_HOLE
- PAGE 60: ADDED A NEW FET CONNECTION CIRCUIT, PP5V_S0_LCD_PWR, J6955 APN 516S0797
- PAGE 60: RENAMED INPUT/OUTPUT NETS OF 5V S0 FET CIRCUITS TO REFLECT RT AND LT (MATCHES UPDATED ALIASES ON PAGE 8)

PAGES SYNCED FROM CASEY HARDY'S AUDIO_MLB SINCE LAST RELEASE 7.5.0
- PG: 67, ADDED =PP3V3_S3_AUDIO NET
- PG: 67, ADDED R6760
- PG: 67, ADDED -XW6792
- PG: 69, ADDED ISNS_ALIAS NOTES
- PG: 69, NO STUFFED R8724

3/29/2009: RELEASE 8.0.0 (RFA)-
- PAGE 7: SCRUBBED THROUGH THE FUNCTIONAL TEST POINTS AGAINST TOM'S SPREADSHEET
- PAGE 7: RENAMED RIGHT CLUTCH CONNECTOR TO X16 WIRELESS CONNECTOR
- PAGE 7: DELETED BATT SIGNAL CONN AND ADDED HALL EFFECT CONNECTOR TEST POINTS
- PAGE 7: ADDED THE NEW TEST POINTS
- PAGE 8: ADDED TP_ALIASES FOR - CARDREADER_RESET, USB_CARDREADER_N/P, AND USB_TR_N/P
- PAGE 9: FIXED BAD TP_NC_NETS -- TP_RTL8211_CLK125, TP_PP3V3_ENET_PHY_VDDREG
- PAGE 41: DELETED 2001Z NLE MOUNTING HOLE AS IT IS NO LONGER NEEDED
- PAGE 34: RENAMED TITLE: RIGHT CLUTCH CONNECTOR TO X16 WIRELESS CONNECTOR
- PAGE 50: REPLACED R5240 WITH APN 114S0236 (3.3K 1% 0L, 1/16W, 0402, 84.50HM RESISTOR)
- PAGE 66: FIXED UNNAMED NETS CONNECTED TO - R6933
- PAGE 74: ADDED XW7401, XW7402, XW7403 AND XW7404
- PAGE 76: FIXED BAD TP_NC_NETS -- TP_PDRREG_PGOOD
- PAGE 78: ADDED PLACEMENT NOTE TO REDRIVER - APN 152S0518
- PAGE 69: CHANGE PIN OUTS OF J6955 AS PER CHINMAY

3/31/2009: RELEASE 9.0.0 (RFA)-
- PAGE 4: DELETED DEBUG_SENSE BOM OPTION AND ADDED MEM SENSE AND 1POS_HIGH_SIDE_SENSE OPTIONS UNDER K84_COMMON_BOM_GROUP
- PAGE 4: ADDED 2 PCS MCP_HIGH_SIDE_SENSE AND 1 PCS MCP_MEM_SENSE BOM OPTIONS UNDER K84_COMMON BOM GROUP
- PAGE 4: ADDED SMCPL POGO PIN 870-1699 AS ALTERNATE FOR THE MEDIUM ONES
- PAGE 4: UPDATED DESCRIPTION FOR TP_TP_PP
- PAGE 4: ADDED 2 PCS OF 10K PU RESISTORS FROM TOM (SPREADSHEET ATTACHED TO THE RADAR)
- PAGE 12: REPLACED C1260 WITH APN 128S0207 AS PER DAYU
- PAGE 12: ADDED PLACEMENT NOTE TO C1260
- PAGE 45: ADDED VOLTAGE = 5V TO THE TEMP SENSOR
- PAGE 55: ADDED 2 OHMS SERIES RESISTOR ON THE MCP SMBUS CONNECTIONS TO MCP SMBUS 0 ASSOCIATED BOM OPTION MCPSMC_DIGITEMP_YES WITH THESE 0 OHMS
- PAGE 55: ADDED 2 OHMS SERIES RESISTOR ON THE MCP SMBUS 1 CONNECTIONS. AND, ASSOCIATED BOM OPTION MCPSMC_DIGITEMP_YES WITH THESE 0 OHMS
- PAGE 55: ADDED 2 OHMS SERIES RESISTOR ON THE MCP SMBUS 0 CONNECTIONS. AND, ASSOCIATED BOM OPTION MCPSMC_DIGITEMP_YES WITH THESE 0 OHMS
- PAGE 55: ADDED 2 OHMS SERIES RESISTOR ON THE MCP SMBUS 1 CONNECTIONS. AND, ASSOCIATED BOM OPTION MCPSMC_DIGITEMP_YES WITH THESE 0 OHMS
- PAGE 52: ADDED BOM OPTION MCPSMC_DIGITEMP NO TO R5230 AND R5231
- PAGE 52: ADDED 2 OHMS SERIES RESISTOR ON THE MCP SMBUS 0 CONNECTIONS. AND, ASSOCIATED BOM OPTION MCPSMC_DIGITEMP_YES WITH THESE 0 OHMS
- PAGE 52: ADDED 2 OHMS SERIES RESISTOR ON THE MCP SMBUS 1 CONNECTIONS. AND, ASSOCIATED BOM OPTION MCPSMC_DIGITEMP_YES WITH THESE 0 OHMS
- PAGE 52: ADDED BOM OPTION MCPSMC_DIGITEMP NO TO R5230 AND R5231
- PAGE 52: UPDATED TO 2.2K PER NEW UPDATES FROM TOM
- PAGE 52: ADDED PLACEMENT NOTE TO R5230 AND R5231
- PAGE 52: FIXED SENSOR ADC SMBUS CONNECTIONS (BOTH SCL AND SDA WERE WRONGLY CONNECTED TO SMB_0_S0_DATA NETS
- PAGE 60: REFRESHED HALL EFFECT SENSOR WITH THE NEW SYMBOL
- PAGE 96: RE-ROUTED LED RETURN SIGNALS DUE TO LAYOUT FEASIBILITY(CHIP WAS MOVED TO TOP SIDE)
- PAGE 90: ADDED C9017 (1000PF) CAP AS PER JOHN SCHEN
- PAGE 97: FIXED THE LCDBKLT_VIN SIGNAL NAME ASSOCIATION TO THE CORRECT NET INSTEAD OF R9730 PIN
- PAGE 97: DISCONNECTED PGND (QE CAPS) FROM XW9780 AND ADDED A SEPARATE XW9701 SHORT TO ISOLATE NOISY GND FROM THE SYSTEM GND NAMES
- PAGE 97: ADDED PGND AND ASSIGNED MIN LENGTH TRACK WITH ATTRIBUTES
- PAGE 97: RENAMED GND_LCDBKLT AND GND_PGND TO GND_LCDBKLT_POND
- PAGE 97: DISCONNECTED PINS 2 AND 5 FROM GND (PINS:13,19,21)AND CONNECTED SEPARATELY TO SYSTEM_GND
- PAGE 97: REPLACED D9710 WITH 40V PART- APN 371S0580 AS PER DEREK
- PAGE 97: STUFFED R9726 AND SWAPPED C9705 AND R9705 AS PER FREESCALE FOR COMPENSATION ALSO, CHANGED R9705 TO 10K 1% VALUE - APN 114S0315

4/2/2009: RELEASE 9.2.0 (MAJOR)-
- PAGE 7: SCRUBBED TO THE LATEST UPDATE FROM TOM
- PAGE 49: FIXED PLACEMENT NOTE ASSOCIATED WITH C4907 (SHOULD BE: PLACE NEAR PIN E1)
- PAGE 49: FIXED PLACEMENT NOTES ASSOCIATED WITH R4989,C4928(SHOULD BE:PLACE NEAR PIN M12)
- PAGE 51: FIXED PLACEMENT NOTE ASSOCIATED WITH R5148 (SHOULD BE:PLACE NEAR PIN AF3)
- PAGE 52: FIXED DUPLICATION OF BAKE BASE TRUE ASSOCIATED WITH SMBUS_SMC_B_S0_SCL/SDA
- PAGE 97: RENAMED SINGLE PIN NET GND_LCDBKLT TO GND_LCDBKLT_POND

SYNC MASTER=K24_MLB SYNC DATE=01/19/2009

PAGE TITLE: Revision History

Apple Inc.

DRAWING NUMBER: 051-7982 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 5 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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Revision History NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

4/2/2009 - RELEASE 9.0.0 (MAJOR):
- PAGE 4:B ADDED 8.95MM SANYO PART 128S0288 AS ALTERNATE TO 128S0271
- PAGE 4:B ADDED 8.95MM SANYO PART 128S0286 AS ALTERNATE TO 128S0248
- PAGE 4:B DELETED 152S0694 ALTERNATE ENTRY FOR 152S0138 AS IT IS NOT USED
- PAGE 5A - REPLACED Q5032 & Q5033 BY THE NEW SINGLE Q5032 & Q5033 (APN 376S0612) NCPD PITS FOR ROUTING PURPOSES (SH_ANODE SIGNAL)
- PAGE 5:E CHANGED R9417 TO 118OHM 1/16W 1% (APN 2M1271)
- PAGE 7:J ADDED MIN_LINE_NECK_WIDTH ATTRIBUTES TO 5V_S3_DRVL, 3V3S5_VBST, 3V3S5_DRVL (FIXED THE NET NAMES ADDED UNDERSCORE)
- PAGE 75: CHANGED L7560 TO APN 152S0526 - 0.68UH, 3.5MOHM 16A - AS PER DAYU
- PAGE 76: CHANGED C7561 TO 1.2UF APN 214S0319 FOR SS1 SINCE THE CORRECT ISET AS PER DAYU
- PAGE 97: CHANGED MIN_NECK_WIDTH ASSOCIATED WITH PPVOUT_S0_LCDBKLT TO 0.24MM AS THAT'S THE PIN WIDTH
- PAGE 97: CHANGED MIN_LINE/NECK_WIDTH ASSOCIATED WITH GND_LCDBKLT_SGND TO 0.6/0.24MM

PAGES SYNCED FROM DAVID'S AUDIO_MLB SINCE LAST RELEASE 9.2.0
- REMOVED R6725 AND =PP3V3_S3_AUDIO CONNECTION TO MAX14504 ANALOG SWITCH

4/2/2009: RELEASE: 9.4.0 (MAJOR):
- PAGE 97: ADDED A 1000PF CAP (C9727) ON LCDBKLT_VIN NEAR PIN 1
- PAGE 97: REPLACED C9717 WITH 1000PF CAP APN 132S0147 AND ADDED PLACEMENT NOTE AS PER JOHN SCHEN

4/2/2009: RELEASE: 9.5.0 (MAJOR):
- PAGE 9: REPLACED Z0900,Z0907,Z0910 AND Z0911 MLB MOUNTING HOLES WITH 2.7 MM DIAMETER PLATED HOLES - APN 998-1584

4/3/2009: RELEASE: 9.6.0 (MAJOR):
- PAGE 1: UNDER K84_PROGPARTS BOM GROUP, REPLACED BLANK P/N WITH PROGRAMMED P/N
- PAGE 8: ADDED GLOBAL _DIGITAL GROUND NET WITH MIN_LINE/NECK_WIDTH AND VOLTAGE ATTRIBUTES
- PAGE 9: REPLACED Z0900 AND Z0913 MLB MOUNTING HOLES WITH 2.7 MM DIAMETER PLATED HOLES - APN 998-1584
- PAGE 9: DELETED GND MIN_LINE/NECK_WIDTH AND VOLTAGE ATTRIBUTES FROM FAN STANDOFF

PAGES SYNCED FROM LENG'S AUDIO_MLB SINCE LAST RELEASE 9.5.0*
- REMOVED ADDITIONAL STUFF AROUND RESISTORS ON ANALOG SWITCH
- CONNECT AUDIO JACK SHIELD TO DIGITAL GROUND.

4/3/2009: RELEASE: 10.0.0 (RFA):
- PAGE 3: ADDED 2X4 TOTAL POGO PINS FOR EMI - 4 STUFFED AT THE BOTTOM, 3 UNSTUFFED ON THE TOP
- PAGE 68: DELETED MAKE_BASE=TRUE ASSOCIATED WITH PCIE_RESET_L
- PAGE 68: FIXED DUPLICATION OF MAKE_BASE=TRUE ASSOCIATED WITH PCIE_RESET_L AND MIKEY_CPU_DP
- PAGE 69: REFRESHED J6955 SYMBOL - APN 516S0787
- PAGE 78: DELETED NOTE ASSOCIATED WITH ALL SYS_PWRGD
- PAGE 78: DELETED SYNONYMS AS THEY ARE NOT NEEDED ANYMORE (DUE TO 0 OHMS)

PAGES SYNCED FROM LENG'S AUDIO_MLB SINCE LAST RELEASE 9.6.0*
- CHANGED 100K PULL-DOWN TO GND ON HP-DET NETS.
- CHANGED MIN_WIDTH TO DOUBLE HP-DET NETS.

4/5/2009: RELEASE 10.1.0 (MAJOR):

- PAGE 4: ADDED CHGR_6258_BOM_OPTION UNDER MODULE PARTS TABLE AND TO K84 MISC BOM GROUP. THIS IS TO STUFF ISL6259 PER DAYU
- PAGE 9: ADDED ONE MORE TALL POGO PIN ON BOTTOM SIDE
- PAGE 33: FIXED THE NOTE ON THE XDP PAGE - REPLACING 920-0620 ADAPTER BOARD WITH 929-0782 ADAPTER FLEX
- PAGE 34: RENAMED PSWLAN_SS_NET TO P3V3WLAN_SS
- PAGE 39: DELETED TEXT NOTE CREATED TO REPLACE R4690 AS IT IS NA TO K84
- PAGE 39: MOVED THE R6251 CONNECTION TO SENSOR ADC TO THE RIGHT SIDE TO SHOW A SEPARATE CONNECTION FOR CLARITY
- PAGE 52: DELETED TEXT NOTE ON BATTERY LED DRIVER AS IT IS NA TO K84
- PAGE 69: PUT R6961 BEFORE C6955 TO GET RC FILTER - ALSO, FOR NOW, REPLACED R6961 WITH A 0 OHM RESISTOR AND NOSTUFF C6955
- PAGE 70: ADDED OMIT BOM OPTION TO U7000 AS THIS PART WILL GET STUFFED WITH EITHER ISL6258 OR ISL6259 DEPENDING UPON PAGE 4 BOM TABLE
- PAGE 70: FIXED Q7001 DRAIN-SOURCE ORIENTATION

4/6/2009 - RELEASE 10.1.1 (MINOR):

SCHEMATIC AND BOM CLEAN-UP
- PAGE 4: DELETED CHGR_6258 AND RENAMED 6259_NO TO CHGR_6259_NO. REPLACED CHGR_6258 WITH CHGR_6259_NO IN MODULE PARTS TABLE
- PAGE 4: DELETED ENTRIES IN THE ALTERNATE BOM TABLE FOR THE FOLLOWING APN: 516-0213 AND 516S0789
- PAGE 8: DELETED =PP3V3_S3_AUDIO ALIAS AS IT IS NO LONGER APPLICABLE
- PAGE 67: DELETED NO_TEST = TRUE ATTRIBUTE FROM J2 SCLK AND J2_MOSI AS THEY CONFLICT WITH FUNC_TEST ATTRIBUTE ON PAGE 7
- PAGE 69: RENAMED 6259_NO/YES TO CHGR_6259_NO/YES

4/6/2009 - RELEASE 11.0.0 (OK2FAB):

- NO CHANGE SINCE LAST MINOR RELEASE 10.1.1

4/7/2009 - RELEASE 12.0.0 OK2FAB (RFA):
**NO RANGE SYNCED LAST RELEASE 12.0.0.
THIS IS A RESUBMIT AS PREVIOUS RFA DIDNT GO THROUGH*

4/23/2009 - RELEASE 12.1.0 (MAJOR):
- PAGE 4: ADDED METAL PART ALTERNATES FOR USB AND MINI DP CONNECTORS. ALSO ADDED CORRESPONDING NOTES.
  514-0690 ALTERNATE FOR 514-0691;
  514-0688 ALTERNATE FOR 514-0689;
- PAGE 39: REPLACED J1300 XDP CONNECTOR WITH MORE ROBUST CONNECTOR APN 083-2515
- PAGE 39: REPLACED J3900 ETHERNET CONNECTOR WITH PORTPLASTIC CONNECTOR APN 514-0692
- PAGE 46: REPLACED J4600 & J4610 USB CONNECTORS WITH PORTPLASTIC CONNECTOR APN 514-0688
- PAGE 75: CHANGE Q7560 AND Q7565 TO SIS426 APN 376S0749 PER RDAR://8812904
- PAGE 75: CHANGE R7565 TO 10MM APN 113S0023 PER RDAR://8812904
- PAGE 78: CHANGED THE CPU_VTT OVER CURRENT TRIP POINT PER RDAR://6792329 BY CHANGING R7004 FROM 0.07KΩ) TO 0.04KΩ)
- PAGE 94: REPLACED J9400 DP CONNECTOR WITH PORTPLASTIC CONNECTOR APN 514-0690
- PAGE 75: CHANGED C7565 AND C7568 TO CASE_B4_SM PACKAGE FROM CASE_B2_SM DUE TO PACKAGING ERROR (SAME APN)

4/24/2009 - RELEASE 12.2.0 (MAJOR):
PAGES SYNCED FROM CASEY'S AUDIO_MLB SINCE LAST RELEASE 12.1.0*
- REPLACED J6700 WITH APN: 514-0694
- ADDED D6702 AND L6708
- CONNECTED R6860 TO AUD_IP_PERPH_DET

4/27/2009 - RELEASE 12.3.0 (MAJOR & WEEKLY ECO):
- PAGE 4: ADDED NEW BOM ENTRY 639-0254 FOR MOLEX DDR3 CONNECTOR CONFIG. ALSO, EDITED 639-0025 BOM NAME TO REFLECT FOXCONN DDR3 CONNECTOR. ADDED TWO ENTRIES (J3200 AND J3100) FOR FOXCONN AND TWO FOR MOLEX MODULE PARTS TABLE
- PAGE 74: CHANGED C7432 TO 0.001UF AS PER RDAR://6792327
- PAGE 74: UNSTUFFED C7434 AS PER RDAR://6792327
- PAGE 74: CHANGED C7428 TO 0.47UF AS PER RDAR://6792327
- PAGE 74: CHANGED R7415 TO 10.5K AS PER RDAR://6792327
- PAGE 97: CHANGED R9716 FROM 226K TO 243K TO CHANGE THE OVP POINT TO 35.3V AS PER KIRAN

4/28/2009: RELEASE 12.4.0 (MAJOR):

- PAGE 67: ADDED 0603_FERRITE PLACEHOLDERS APN 155S0367 ON RIGHT PIEZO SPEAKER FOR EMI PURPOSES - L6707 & L6708

4/28/2009: RELEASE 12.5.0 (MAJOR):
- PAGE 67: MOVED L6707 & L6708 TO J6703 (FULL RANGE SPEAKER CONNECTOR) BETWEEN CAPS AND CONNECTOR

4/29/2009: RELEASE 12.6.0 (MAJOR & WEEKLY ECO):

- PAGE 67: ADDED 0603_FERRITE PLACEHOLDERS APN 155S0367 ON RIGHT PIEZO SPEAKER FOR EMI PURPOSES - L6707 & L6708
- PAGE 97: CHANGED L9710 TO A BIGGER 2525 PACKAGE (LOW DCR) APN 152S0585 FOR BETTER EFFICIENCY

4/29/2009: RELEASE 12.7.0 (MAJOR & WEEKLY ECO):
- PAGE 97: CHANGED L9710 BACK TO THE ORIGINAL APN 152S0826 AS 2525 PACKAGE CAN'T FIT IN

5/01/2009: RELEASE 12.8.0 (MAJOR):
- PAGE 4: ADDED A36 FEE NUMBER FOR NEW BOM CONFIGURATION 639-0254
- PAGE 60: ADDED 8 OHMS SERIES RESISTORS R6003 AND R6004 ON AVDD AND DVDD SUPPLY RAILS TO ADC CHIP
- PAGE 60: CHANGED R6001 & R6002 TO 33 OHMS RESISTORS TO FIX UNDERSHOOT ON I2C BUS

05/01/2009: RELEASE 12.9.0 (MAJOR):
- PAGE 4: UPDATED PLASTIC PART ALTERNATES FOR USB AND MINI DP CONNECTORS. ALSO ADDED CORRESPONDING NOTES.
  514-0690 PLASTIC ALTERNATE FOR 514-0691 METAL;
  514-0688 PLASTIC ALTERNATE FOR 514-0689 METAL'

- PAGE 46: REPLACED PLASTIC USB CONNECTORS WITH METAL APN 514-0689 PARTS
- PAGE 94: REPLACED PLASTIC MINI DP CONNECTOR WITH METAL APN 514-0691 PART

05/04/2009: RELEASE 12.10.0 (MAJOR):
- PAGE 4: REMOVED SHORT POGO PIN ALTERNATE
- PAGE 4: REVERTING MCP TO EARLIER USE APN 338S0710
- PAGE 60: CHANGED U6050 INA 211 PART TO 200X DATSHEET INA 210 APN 353S2073

05/05/2009: RELEASE 12.11.0 (MAJOR & WEEKLY ECO):
- PAGE 4: ADDED 4 QUANTITIES OF DIMM CONNECTOR SCREWS APN 452-1708
- PAGE 46: ADDED NOTE ABOUT USING METAL PART'S SCHEMATIC AND CAD SYMBOLS THOUGH FOR IS PLASTIC USB CONNECTOR PART
- PAGE 94: ADDED NOTE ABOUT USING METAL PART'S SCHEMATIC AND CAD SYMBOLS THOUGH FOR IS PLASTIC MINI DP CONNECTOR PART

05/08/2009: RELEASE 12.12.0 (MAJOR & WEEKLY ECO):

- PAGE 4: DELETED 2X4 TOTAL POGO PINS FOR 128S0248 & 128S0271 FROM THE ALTERNATE TABLE AS THEY ARE NOT USED
- PAGE 4: TURNING ON BOM OPTION VERSMC_DIGITEMP (YES AS POR IS TO CONNECT MAKEY TO MCP79 SMBUS 0 INSTEAD OF SMBUS 1 AND TO CONNECT TAC & NB_THERM TO SMBUS 1
- PAGE 4: ADDED A TEXT NOTE STATING THAT ADC CAN ONLY WORK IN S0 STATE AS PER DAYU
- PAGE 72: CHANGED C3714 AND C3715 TO 2.2UF APN 138S0642 TO FIX ETHERNET JITTER ISSUE
- PAGE 60: CHANGED R5030 TO 63.4 OHMS APN 114S0102 TO INCREASE THE SIL CURRENT PER RDAR:/6808LEW/6767822
- PAGE 59: CHANGED R5714 TO 0 OHM APN 116S0004 PER RDAR:/7PROBLEM/6753625
- PAGE 52: CHANGED R5280, R5291, R5290 & R5261 TO 2K APN 116S0073
- PAGE 72: REPLACED C7252, C7291 & C7292 WITH 5.95MM SANYO APN 128S0288
- PAGE 72: REPLACED C7240 & C7282 WITH 5.95MM SANYO APN 128S0286
- PAGE 73: REPLACED C7331 & C7345 WITH 5.95MM SANYO APN 128S0286
- PAGE 77: CHANGED C7771 TO 47UF APN 138S0659 TO FIX ETHERNET JITTER ISSUE

05/10/2009: RELEASE 12.13.0 (MAJOR & WEEKLY ECO THRU' EMAIL):
- PAGE 60: CHANGED R6003 AND R6004 TO 10 OHMS 5% RESISTOR VALUES RDAR:7PROBLEM/6834630

05/11/2009: RELEASE 12.14.0 (MAJOR & WEEKLY ECO - THRU' EMAIL):

- PAGE 57 : CHANGED R5714 TO 165 OHMS APN 114S0141 AS PER RDAR:/7PROBLEM/6875543
- PAGE 72 : CHANGED C7252, C7291 & C7292 BACK TO ORIGINAL APN 128S0271

05/20/2009: AGILE RELEASE PROTO 2 OK2FAB 13.0.0 (FAB):

- FINAL PROTO 2 OK2FAB RELEASE
- UPDATED PAGE BORDERS TO NEW E4 DSIZE STANDARDS

05/22/2009: AGILE RELEASE PROTO 2 OK2FAB 14.0.0 (FAB)-

- **RETRY***
- FINAL PROTO 2 OK2FAB RELEASE
- UPDATED PAGE BORDERS TO NEW E4 DSIZE STANDARDS

06/09/2009: RELEASE 14.1.0 (MAJOR)-
- PAGE 4: REMOVING CHGR_6259_NO_BOM_OPTION AS ISL 6259 IS NOT POR
- PAGE 4: ADDED NEW ISL PART APN 353S2718 AS AN ALTERNATE TO FIX B4 DONGLE ISSUE
- PAGE 5: REPLACED ALL MEDIUM POGO PINS WITH APN 870-1794 (2 MM) AND 6592-165 POGO PINS WITH APN 870-1795 (4.7 MM) ONLY
- PAGE 59: ADDED R5922 10 OHMS SERIES R ON VDD SUPPLY TO FIX SMS NOISE ISSUE
- PAGE 62: REMOVED C6784 & C6785 FROM CONNECTOR RES0870
- PAGE 70: REMOVED C7008 & C7009 FROM PAGE 4 BOM ATTRIBUTES AS ISL 6259 IS NOT POR
- PAGE 78: REPLACED R7051 & R7053 CHGR_6259_YES BOM OPTIONS COMPONENTS WITH XW SHORTS- XW7052 & XW7054
- PAGE 78: REPLACED R7052 & R7054 CHGR_6259_NO BOM OPTION COMPONENTS WITH XW SHORTS- XW7052 & XW7054
- PAGE 78: REPLACED R7053 & R7054 CHGR_6259_YES BOM OPTIONS COMPONENTS
- PAGE 97: CHANGED C9480 TO 220UF (APN 138S0661) & CHANGED C9480 TO 220UF (APN 138S0654): TO FIX B4 DONGLE ISSUE

PAGES SYNCED FROM CASEY HARRIGAN'S AUDIO_MLB SINCE LAST RELEASE 14.0.0*
- ADDED R9862 PULL-UP RESISTOR TO PERPH_DETECT CKT.

06/10/2009: RELEASE 14.2.0 (MAJOR)-

- PAGE 4: ADDED APN 138S0661 LOW NOISE MURATA CAPS AS ALTERNATE FOR C9715 & C9716 TO FIX LCD BKLT AUDIBLE NOISE ISSUE
- PAGE 48: ADDED 8.10F CAPS ON SMS_X_AXIS, SMS_Y_AXIS & SMS_Z_AXIS NETS TO FIX NOISE ISSUE
- PAGE 77: CHANGED R7780 TO 25.5K APN 114S0354 & R7781 TO 80.6K APN 114S0402 AS PER DAYU

06/11/2009: RELEASE 14.3.0 (MAJOR)-
- PAGE 77: ADDED 0 OHMS BOM OPTIONS R7782 BETWEEN PIN 4 OF U7750 (SKIP PIN) AND POWER RAIL AND R7783 BETWEEN PIN 4 AND GND. R7782 WILL BE NOSTUFF FOR NOW. THIS IS AS PER DAYU TO FIX ETHERNET JITTER ISSUE

06/11/2009: RELEASE 14.4.0 (MAJOR)-
- PAGE 49: REPLACED C4950-C4952 WITH 1UF APN 138S0640 CAPS
- PAGE 78: DISCONNECTED PVDD5_S5_PGOOD FROM PIN 3 OF U7640 AND CONNECTED IT TO PIN 1 (RSMRST_PWRGD) TO FIX LEAKAGE ISSUE

06/12/2009: RELEASE 14.5.0 (MAJOR)-
- PAGE 9: ADDED ONE MORE EXTRA TALL POGO PIN AS PER EMC RECOMMENDATION : 5S0020
- PAGE 78: ADDED 0 OHM BOM OPTION R7895 BETWEEN 1V05_S5_PGOOD AND RSMRST_PWRGD FOR DEBUG PURPOSES

06/22/2009: RELEASE 14.6.0 (MAJOR)-

- PAGE 4: ADDED CPU APN 337S3769 AS ALTERNATE TO 337S3704
- PAGE 4: ADDED NOSTUFF BOM OPTION TO 2S0920
- PAGE 59: CHANGED R6029 TO 49.9 OHMS APN 114S0091 (KB_LCD_CURRENT TO 12MA)
- PAGE 97: ADDED INITIAL TITLE BLOCK TO C9715-C9718
- PAGE 97: CHANGED R9710 TO 7.68K APN 114S0304 (LCD_BKLT CURRENT TO 20MA)

06/25/2009: RELEASE 14.7.0 (MAJOR)-

- PAGE 70: DELETED OMIT BOM OPTION FROM U7000 AS ISL6259 HAVE BEEN REMOVED

07/17/2009: AGILE EVT OK2FAB RELEASE 15.0.0 (FAB)-

- NO CHANGES SINCE LAST MAJOR 14.7.0. THIS IS FINAL EVT FAB RELEASE

07/21/2009: RELEASE 15.1.0 (MAJOR)-

- PAGE 4: DELETED MIKEY_LOAD_DET BOM OPTION FROM THE TABLE UNDER K84_MISC CATEGORY AS PER CASEY
- PAGE 4: UPDATED ALTERNATES FOR MINI DP AND USB CONNECTORS WITH PG2 PLASTIC CONNECTORS - APN 514-0708 (MDP) & 514-0705 (USB) AND, UPDATED NOTE BELOW THE ALTERNATES PARTS TABLE ACCORDINGLY
- PAGE 4: ADDED PG2 CONNECTOR APN 514-0704 IN THE MODULE PARTS TABLE FOR RJ45 J3900 CONNECTOR
- PAGE 4: DELETED 353S2310 PART FROM THE ALTERNATES BOM TABLE AS ALL PRODUCTION HAS NOW MOVED TO ITS ALTERNATE PART 353S2718
- PAGE 4: ADDED NEW INTERSIL PART APN 353S2718 IN THE MODULE PARTS TABLE FOR U7870 TO FIX B4 DONGLE ISSUE
- PAGE 11: DELETED NOSTUFF BOM ATTRIBUTE FROM R2143 AS MIKEY_LOAD_DET CIRCUIT HAS BEEN REMOVED. SO R2143 NEEDS TO BE STUFFED NOW.
- PAGE 39: ADDED BOMOPTION ATTRIBUTE OMIT TO J3900 AS NEW PG2 CONNECTOR PART HAS BEEN ADDED ON PAGE 4 MODULE PARTS TABLE
- PAGE 78: ADDED BOMOPTION ATTRIBUTE OMIT TO U7870 AS NEW INTERSIL PART PART HAS BEEN ADDED ON PAGE 4 MODULE PARTS TABLE

07/27/2009: RELEASE 15.2.0 (MAJOR):
- PAGE 11: DELETED LOW NOISE MURATA CAP ENTRY FROM THE ALTERNATES TABLE
- PAGE 49: CHANGED SMS NOISE FILTERING CAPS C4950-C4952 TO 0.47UF APN 132S0178 TO FIX THE SMART SLEEP FAILURE
- PAGE 78: DISCONNECTED PVDD5_S5_PGOOD FROM PIN 4 (VREF) AS IT WAS INCORRECTLY CONNECTED. THEREBY CAUSING HIGHER SLEEP/SHUTDOWN POWER
- PAGE 78: NOSTUFFED C9715 AND CHANGED C9716 TO APN 138S0661 AS POR IS TO HAVE SINGLE CAP LOW NOISE MURRATA CAP SOLUTION AS PER ACOUSTICS ENGINEER

08/05/2009: RELEASE 15.3.0 (MAJOR):
- PAGE 4: ADDED APN 138S0608 (TAIYO-YUDEN) AS AN ALTERNATE FOR APN 138S0602
- PAGE 4: ADDED PDNI_GOLD_PLATED AUDIO CONNECTOR W/ CHAMFER APN 514-0718 AS AN ALTERNATE FOR 3070W GOLD PLATED AUDIO
- PAGE 4: ADDED GOLD PLATED AUDIO CONNECTOR W/O CHAMFER APN 998-2622 AS AN ALTERNATE FOR 3070W GOLD PLATED AUDIO
- PAGE 4: ADDED GOLD PLATED RJ45 CONNECTOR APN 998-2621 AS AN ALTERNATE FOR J3900 APN 514-0704
- PAGE 4: ADDED GOLD PLATED MINI DP CONNECTOR APN 998-2626 AS AN ALTERNATE FOR J4400 APN 514-0691
- PAGE 4: ADDED GOLD PLATED USB CONNECTOR APN 998-2624 AS AN ALTERNATE FOR J4800/J4810 APN 514-0689
- PAGE 4: ADDED LOW NOISE POGO PINS 870-1885 (MEDIUM), 870-1886 (TALL), AND 870-1887 (THIN) AS ALTERNATES
- PAGE 49: CHANGED C4950, C4951, C4952 TO APN:132S0131 (CAP,0402,0.033UF, 16V,10%) AS THESE WOULD BE USED TO ACHIEVE CUT-OFF FREQUENCY OF 110KHZ FOR SMS (AS PER THE VENDOR) AND FILTER THE NOISE TOO AS SEEN BY SMC CHIP - CAPS ON SMS PAGE WOULD BE UNSTUFFED
- PAGE 59: ADDED NOSTUFF BOM OPTION ATTRIBUTE TO C5923-C5925 AS STATED ABOVE- ALSO, EDITED THE NOTE ACCORDINGLY
- PAGE 70: CHANGED R7031 FROM 10 OHM TO 2.2 OHM, 5%, APN:116S0010 TO FIX SLOW CHARGING ISSUE - PER DAYU
- PAGE 70: CHANGED R7047 FROM 10 OHM TO 0 OHM, 5%, APN:116S0004 TO FIX SLOW CHARGING ISSUE - PER DAYU
- PAGE 70: CHANGED C7043 FROM 0.1UF TO 1UF, 10%, APN:138S0640 TO FIX SLOW CHARGING ISSUE, PER DAYU

08/27/2009: AGILE PDFC OK2FAB RELEASE 16.0.0 (FAB)-

- FINAL PDFC (PRE DVT) RELEASE!
- PAGE 97: REFRESHED THE SYMBOL OF C9715 4.7UF APN 138S0661

08/31/2009: RELEASE 16.1.0 (MAJOR)-

- PAGE 4: REMOVED 138S0606 FROM THE ALTERNATES TABLE AS IT DOESN'T PERTAIN TO K84
- PAGE 4: REPLACED CPU APN 337S3704 WITH 337S3769 IN MODULE PARTS TABLE AND REMOVED 337S3704 FROM THE ALTERNATE PART TABLE FOR 15-337S3769 (P7550)
- PAGE 4: REMOVED 870-1794, 870-1698 & 870-1820 FROM THE ALTERNATES TABLE AS POR IS LOW NOISE POGO PINS
- PAGE 4: ADDED LOW NOISE POGO APNS 870-1885 (IN PLACE OF 870-1794), 870-1886 (IN PLACE OF 870-1698) & 870-1887 (IN PLACE OF 870-1820) IN MODULE PARTS TABLE
- PAGE 4: ADDED NEW INTERSIL ISL62584 (WITH IMPROVED CHARGE CURRENT ACCURACY LIMITS) APN 353S2812 AS ALTERNATE FOR APN 353S2632
- PAGE 4: REMOVED 998S APN FROM THE ALTERNATES TABLE PERTAINING TO I/O CONNECTORS AS THEY ARE NO LONGER FOR POR DVT
- PAGE 4: REMOVED 514-0706, 514-0705 AND 514-0708 FROM THE ALTERNATES TABLE AND ADDED PG2 MODULE PARTS TABLE AS THEY ARE NOW FOR I/O CONNECTORS
- PAGE 9: ADDED OMIT BOM OPTION ON ALL THE POGO PINS
- PAGE 46: ADDED OMIT BOM OPTIONS TO J4600 & J4610 USB CONNECTORS
- PAGE 67: ADDED OMIT BOM OPTION TO J6700 AUDIO CONNECTOR
- PAGE 94: ADDED OMIT BOM OPTION TO J9400 MINI DP CONNECTOR
- PAGE 97: UPDATED SCHEMATIC NOTE RELATED TO TARGET AND ACTUAL ISET & OVP NUMBERS AS PER KIRAN'S EMAIL

09/16/2009: RELEASE 17.0.0 (FAB)-

- FINAL DVT OK2FAB RELEASE

09/21/2009: RELEASE A.0.0 (FAB)-

- FINAL PVT OK2FAB RELEASE
- PAGE 4: ADDED APN 104S0033 (6.8 OHMS, 1/4W) RESISTORS IN MODULE PARTS TABLE FOR R6614, R6631, R6632 & R6633
  ADDED APN 51S6574 FOR XDP CONNECTOR J1300 (TO REPLACE 998-2515)
- PAGE 13: ADDED OMIT TO J1300
- PAGE 56: CHANGED R5030 SIL RESISTOR TO 80.6 OHMS APN 114S0112 AS PER ID
- PAGE 53: REPLACED APN 376S0545 WITH 376S0820 @ QS315 - PER ECO#090727172
- PAGE 66: ADDED BOMOPTION OMIT TO RESISTORS R6612, R6617, R6630 & R6633

10/12/2009: RELEASE B.0.0 (FAB)-

- PROD DEBUG (POST FIRST 5K UNITS 1 MONTH INTO PRODUCTION) OK2FAB RELEASE
- PAGE 4: ADDED NEW BOM GROUPS 639-0594, 639-0555 AND 1 NEW DEVELOPEMENT BOM 639-1076 FOR INITIAL PROTO BOMS
- PAGE 4: UPDATED BOM GROUPS TABLE TO REFLECT AFOREMENTIONED CHANGES. NEW DEVELOPEMENT BOM NOW HAS XDP CONNECTOR AND LOCPLUS COMPONENTS
- PAGE 4: ADDED 6 NEW ENTRIES TO ALTERNATES WITH AFOREMENTIONED NEW 639 BOMS
- PAGE 9: DELETE 8S0000 ENTRY FROM THE EXTERNALS TABLE
- PAGE 70: REPLACED C7088 WITH THE NEW INTERSIL SCREENED PARTS APN 353S2811

11/04/2009 - RELEASE C.0.0 (FAB):
- PROD (POST 1ST MONTH OF PRODUCTION) OK2FAB RELEASE
- PAGE 2: UPDATED SYSTEM BLOCK DIAGRAM
- PAGE 3: UPDATED POWER BLOCK DIAGRAM
- PAGE 4: UPDATED BOM TABLES TO NOT INCLUDE ANY 085 DEVELOPMENT BOMS. AND, K84_DEBUG_PROD BOM GROUP IS TURNED ON

SYNC MASTER=K24_MLB	SYNC DATE=01/19/2009
PAGE TITLE: Revision History	
Apple Inc.	DRAWING NUMBER: 051-7982 SIZE: D
	REVISION: C.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH
	PAGE: 6 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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Functional Test Points

FAN CONNECTORS FUNC_TEST

1116	TRUE	PP5VRT_S0	7 8
1115	TRUE	FAN_RT_PWM	43
1118	TRUE	FAN_RT_TACH	43

(NEED TO ADD 1 GND TP)

MIC FUNC_TEST

1035	TRUE	BI_MIC_LO	53 54
1034	TRUE	BI_MIC_HI	53 54
1036	TRUE	BI_MIC_SHIELD	53 54

SPEAKER FUNC_TEST

1227	TRUE	SPKRAMP_L_N_OUT	52 53
1226	TRUE	SPKRAMP_L_P_OUT	52 53
1228	TRUE	SPKRAMP_R_N_OUT	52 53
1230	TRUE	SPKRAMP_R_P_OUT	52 53
1229	TRUE	SPKRAMP_SUB_N_OUT	52 53
1231	TRUE	SPKRAMP_SUB_P_OUT	52 53

LVDS FUNC_TEST

1016	TRUE	PP3V3_LCDVDD_SW_F	7 65 (NEED 2 TP)
1017	TRUE	PP3V3_S0_LCD_F	65
1018	TRUE	PPVOUT_S0_LCDBKLT	7 47 65 68 (NEED 2 TP)
1019	TRUE	LVDS_IG_DDC_CLK	18 65
1020	TRUE	LVDS_IG_DDC_DATA	18 65
1021	TRUE	LVDS_IG_A_DATA_N<0>	18 65 72
1022	TRUE	LVDS_IG_A_DATA_P<0>	18 65 72
1023	TRUE	LVDS_IG_A_DATA_N<1>	18 65 72
1024	TRUE	LVDS_IG_A_DATA_P<1>	18 65 72
1025	TRUE	LVDS_IG_A_DATA_N<2>	18 65 72
1026	TRUE	LVDS_IG_A_DATA_P<2>	18 65 72
1027	TRUE	LVDS_IG_A_CLK_F_N	65 72
1028	TRUE	LVDS_IG_A_CLK_F_P	65 72
1029	TRUE	LED_RETURN_1	65 68
1030	TRUE	LED_RETURN_2	65 68
1031	TRUE	LED_RETURN_3	65 68
1032	TRUE	LED_RETURN_4	65 68
1033	TRUE	LED_RETURN_5	65 68
1040	TRUE	LED_RETURN_6	65 68
1039	TRUE	PP5V_S3_CAMERA_F	7 65
1037	TRUE	USB_CAMERA_CONN_P	65 73
1038	TRUE	USB_CAMERA_CONN_N	65 73

(NEED TO ADD 5 GND TP)

SATA ODD CONN FUNC_TEST

1204	TRUE	PP5V_SW_ODD (NEED 2 TP)	7 34 47
1205	TRUE	SMC_ODD_DETECT	34 36
1206	TRUE	SATA_ODD_D2R_C_P	34 72
1207	TRUE	SATA_ODD_D2R_C_N	34 72
1208	TRUE	SATA_ODD_R2D_P	34 72
1209	TRUE	SATA_ODD_R2D_N	34 72

(NEED TO ADD 2 GND TP)

SATA HDD/SIL FUNC_TEST

1315	TRUE	PP5V_S0_HDD_FLT (NEED 2 TP)	7 34
1314	TRUE	SATA_HDD_R2D_P	34 72
1316	TRUE	SATA_HDD_R2D_N	34 72
1318	TRUE	SATA_HDD_D2R_C_P	34 72
1317	TRUE	SATA_HDD_D2R_C_N	34 72
1367	TRUE	SYS_LED_ANODE_R	34

(NEED TO ADD 3 GND TP)

BATT POWER CONN FUNC_TEST

1322	TRUE	SMBUS_SMC_BSA_SCL	39 75
1323	TRUE	SMBUS_SMC_BSA_SDA	39 75
1325	TRUE	SYS_DETECT_L	55
1326	TRUE	BATT_POS_F	55 56 (NEED 2 TP)

(NEED TO ADD 2 GND TP)

HALL EFFECT CONNECTOR FUNC_TEST

1328	TRUE	PP3V42_G3H	7 8
1329	TRUE	SMC_LID_R	55

X16 WIRELESS CONN FUNC_TEST

1303	TRUE	PP3V3_S3_BT_F	30
1301	TRUE	CONN_PCIE_MINI_D2R_P	30 72
1302	TRUE	CONN_PCIE_MINI_D2R_N	30 72
1300	TRUE	CONN_PCIE_MINI_R2D_P	30 72
1299	TRUE	CONN_PCIE_MINI_R2D_N	30 72
1228	TRUE	PCIE_CLK100M_MINI_CONN_P	30 72
1223	TRUE	PCIE_CLK100M_MINI_CONN_N	30 72
1288	TRUE	PP3V3_WLAN	7 30 (NEED 2 TP)
1222	TRUE	PCIE_WAKE_L	17 30
1225	TRUE	CONN_USB2_BT_P	30 73
1290	TRUE	CONN_USB2_BT_N	30 73
1271	TRUE	MINI_CLKREQ_Q_L	30
1289	TRUE	MINI_RESET_CONN_L	30

(NEED TO ADD 2 GND TP)

IPD_FLEX_CONN FUNC_TEST

1375	TRUE	PP3V3_S3_LDO	7 45
1374	TRUE	PP18V5_S3	7 45
1372	TRUE	Z2_CS_L	44 45
1376	TRUE	Z2_DEBUG3	44 45
1373	TRUE	Z2_MOSI	44 45
1262	TRUE	Z2_MISO	44 45
1260	TRUE	Z2_SCLK	44 45
1261	TRUE	Z2_BOOST_EN	45
1266	TRUE	Z2_HOST_INTN	44 45
1265	TRUE	Z2_CLKIN	44 45
1263	TRUE	Z2_KEY_ACT_L	44 45
1264	TRUE	Z2_RESET	44 45
1357	TRUE	PSOC_MISO	44 45
1358	TRUE	PSOC_MOSI	44 45
1359	TRUE	PSOC_SCLK	44 45
1357	TRUE	SMBUS_SMC_A_S3_SDA	39 75
1358	TRUE	SMBUS_SMC_A_S3_SCL	39 75
1377	TRUE	PSOC_F_CS_L	44 45
1378	TRUE	PICKB_L	44 45

(NEED TO ADD 2 GND TP)

KEYBOARD CONN FUNC_TEST

1354	TRUE	PP3V3_S3	7 8
1355	TRUE	PP3V42_G3H	7 8
1344	TRUE	WS_KBD1	44
1345	TRUE	WS_KBD2	44
1346	TRUE	WS_KBD3	44
1347	TRUE	WS_KBD4	44
1349	TRUE	WS_KBD5	44
1348	TRUE	WS_KBD6	44
1360	TRUE	WS_KBD7	44
1362	TRUE	WS_KBD8	44
1361	TRUE	WS_KBD9	44
1363	TRUE	WS_KBD10	44
1327	TRUE	WS_KBD11	44
1326	TRUE	WS_KBD12	44
1329	TRUE	WS_KBD13	44
1343	TRUE	WS_KBD14	44
1342	TRUE	WS_KBD15_CAP	44
1341	TRUE	WS_KBD16_NUM	44
1339	TRUE	WS_KBD17	44
1340	TRUE	WS_KBD18	44
1338	TRUE	WS_KBD19	44
1336	TRUE	WS_KBD20	44
1337	TRUE	WS_KBD21	44
1333	TRUE	WS_KBD22	44
1335	TRUE	WS_KBD23	44
1334	TRUE	WS_KBD_ONOFF_L	44
1332	TRUE	WS_LEFT_SHIFT_KBD	44
1330	TRUE	WS_LEFT_OPTION_KBD	44
1331	TRUE	WS_CONTROL_KBD	44

(NEED TO ADD 1 GND TP)

POWER NETS FUNC_TEST

1297	TRUE	PPVCORE_S0_CPU	8
1298	TRUE	PPVCORE_S0_MCP	8
1294	TRUE	PP0V75_S0	8
1296	TRUE	PP1V05_S0	8
1291	TRUE	PP1V5_S0	8
1292	TRUE	PP1V8_S0	8
1293	TRUE	PP5VLT_S0	8
1295	TRUE	PP5VRT_S0	7 8
1283	TRUE	PP3V3_S0	8
1284	TRUE	PP1V5_S3	8
1285	TRUE	PP3V3_S3	7 8
1286	TRUE	PP5V_S3	8
1287	TRUE	PP1V1R1V05_S5	8
1273	TRUE	PP3V3_S5	8
1274	TRUE	PP3V42_G3H	7 8
1275	TRUE	PPBUS_G3H	8
1276	TRUE	PP3V3_ENET_PHY	8
1277	TRUE	PP1V2R1V05_ENET	8
1278	TRUE	PP3V3_G3_RTC	21 22 25
1279	TRUE	PP3V3_WLAN	7 30
1280	TRUE	PP5V_SW_ODD	7 34 47
1281	TRUE	PP5V_S0_HDD_FLT	7 34
1282	TRUE	PP3V3_S5_AVREF_SMC	36 37
1308	TRUE	PP18V5_S3	7 45
1307	TRUE	PP3V3_S3_LDO	7 45
1306	TRUE	PP3V3_LCDVDD_SW_F	7 65
1305	TRUE	PPVOUT_S0_LCDBKLT	7 47 65 68
1304	TRUE	PP4V5_AUDIO_ANALOG	49
1302	TRUE	SMC_PM_G2_EN	36 57 63
1301	TRUE	PM_SLP_S4_L	21 36 37 63
1300	TRUE	PM_SLP_S3_L	21 32 36 63 67
1297	TRUE	PP5V_S3_CAMERA_F	7 65

(NEED TO ADD 1 GND TP)

DC POWER CONN FUNC_TEST

1312	TRUE	PP18V5_DCIN_FUSE (NEED 2 TP)	55
1311	TRUE	ADAPTER_SENSE	55

(NEED TO ADD 2 GND TP)

SYNC MASTER=K24 MLB SYNC DATE=02/04/2009

PAGE TITLE: FUNC TEST

Apple Inc.

DRAWING NUMBER: 051-7982 SIZE: D

REVISION: C.0.0

BRANCH

PAGE: 7 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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"S0,S0M" RAILS

59 =PPVCORE_S0_CPU_REG
(CPU VCORE PWR)
PPVCORE_S0_CPU 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.3 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE
=PPVCORE_S0_CPU 11 12
=PPVCORE_S0_CPU_VSENSE 40

61 =PPCPUVTT_S0_REG
PP1V05_S0 7
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_CPU 10 11 12 13
=PP1V05_S0_MCP_FSB 14 22 23
=PP1V05_S0_MCP_PEX_DVDD 8 23
=PP1V05_S0_MCP_AVDD_UF 23
=PP1V05_S0_MCP_SATA_DVDD 8 23
=PP1V05_S0_MCP_HDMI_VDD 18 24
=PP1V05_S0_VMON 63
=PP1V05_S0_MCP_PLL_UF_R 62

60 =PPMCPCORE_S0_REG
(MCP VCORE AFTER SENSE RES)
PPVCORE_S0_MCP 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PPVCORE_S0_MCP 22 23
=PPVCORE_S0_MCP_VSENSE 40

58 =PP0V75_S0_REG
PP0V75_S0 7
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE
=PPVTT_S0_VTTCLAMP 64
=PP0V75_S0_MEM_VTT_A 27
=PP0V75_S0_MEM_VTT_B 28

64 =PP1V5_S0_FET
PP1V5_S0 7
MIN_LINE_WIDTH=1.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S0_CPU 11 12
=PP1V5_S0_VMON 63
=PP1V8R1V5_S0_MCP_MEM 16 23
=PP1V5_S0_MEM_MCP 28
=PP1V5_S0_MCP_PLL_VLDO 62

62 =PP1V8_S0_REG
PP1V8_S0 7
MIN_LINE_WIDTH=0.10MM
MIN_NECK_WIDTH=0.10MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP3V3R1V8_S0_MCP_IFP_VDD 18 24
=PP1V8_S0_AUDIO 49

62 23 =PP1V05_S0_MCP_PLL_UF
PP1V05_S0_MCP_PLL_UF
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE

64 =PP5VRT_S0_FET
PP5VRT_S0 7
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S0_CPUVTTS0 61
=PP5V_S0_LPCPLUS 38
=PP5V_S0_FAN_RT 43
=PP5V_S0_CPU_IMVP 59

64 =PP5VLT_S0_FET
PP5VLT_S0 7
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S0_DP_AUX_MUX 66
=PP5V_S0_HDD 34
=PP5V_S0_MCPREG 60
=PP5V_S0_VMON 63

64 =PP3V3_S0_FET
PP3V3_S0 7
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S0_XDP 13
=PP3V3_S0_MCP 21 22 23
=PP3V3_S0_MCP_DAC_UF 24
=PP3V3_S0_MCP_VPLL_UF 24
=PP3V3_S0_ODD 34
=PP3V3_S0_SMBUS_SMC_0_S0 39
=PP3V3_S0_SMBUS_SMC_B_S0 39
=PP3V3_S0_SMBUS_MCP_0 39
=PP3V3_S0_FAN_RT 43
=PP3V3_S0_AUDIO 49 53 54
=PP3V3_S0_IMVP 59
=PP3V3_S0_LCD 65
=PP3V3_S0_MCP_GPIO 18 19 21
=PP3V3_S0_MCP_PLL_UF 23
=PP3V3R1V5_S0_MCP_HDA 21 23
=PP3V3_S0_SMC 37
=PP3V3_S0_MCPTHMSNS 42
=PP3V3_S0_CPUTHMSNS 42
=PP3V3_S0_DPCONN 67
=PPSPD_S0_MEM_A 27
=PPSPD_S0_MEM_B 28
=PP3V3_S0_PWRCTL 63
=PP3V3_S0_VMON 63
=PP3V3_S0_CPUVTTISNS 41
=PP3V3_S0_SMBUS_MCP_1 39
=PP3V3_S0_P1V8S0 62
=PP3V3_S0_MCP_PLL_VLDO 62
=PP3V3_S0_MCPDDRISNS 41

"S3" RAILS

58 =PP1V5_S3_REG
PP1V5_S3 7
MIN_LINE_WIDTH=1.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S3_P1V5S0FET 64
=PP1V5_S3_MEM_A 27
=PP1V5_S3_MEM_B 28
=PP1V5_S3_MEMRESET 29

64 =PP3V3_S3_FET
PP3V3_S3 7
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S3_SMBUS_SMC_A_S3 39
=PP3V3_S3_PDCISENS 58
=PP3V3_S3_SMBUS_SMC_MGMT 39
=PP3V3_S3_VREFMRGN 26
=PP3V3_S3_WLAN 30
=PP3V3_S3_MCP_GPIO 21
=PP3V3_S3_TPAD 44
=PP3V3_S3_SMS 46
=PP3V3_S3_BT 30

57 =PP5V_S3_REG
PP5V_S3 7
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S3_EXTUSB 35
=PP5V_S3_CAMERA 65
=PP5V_S3_AUDIO_AMP 52
=PP5V_S3_MCPDDRFET 64
=PP5V_S3_1V5S30V75S0 58
=PP5V_S3_AUDIO 49 51 53
=PP5V_S3_P5VLTS0FET 64
=PP5V_S3_VTTCLAMP 64
=PP5V_S3_DEBUG_ISNS 47
=PP5V_S3_SYSLED 37
=PP5V_S3_TPAD 45
=PP5V_S3_ODD 34
=PP5V_S3_DEBUG_ADC_AVDD 47
=PP5V_S3_DEBUG_ADC_DVDD 47
=PP5V_S3_P5VRTS0FET 64

58 26 =PPVTT_S3_DDR_BUF
PPVTT_S3_DDR_BUF
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.75V
MAKE_BASE=TRUE

"S5" RAILS

62 =PP1V05_S5_REG
PP1V1R1V05_S5 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S5_MCP_VDD_AUXC 22 23
=PP1V05_ENET_P1V05ENETFET 32

57 =PP3V3_S5_REG
PP3V3_S5 7
MIN_LINE_WIDTH=1.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S5_MCP_GPIO 18 20
=PP3V3_S5_ROM 38 48
=PP3V3_S5_LCD 65
=PP3V3_S5_MCP 22 23
=PP3V3_S5_MCPPWRGD 25
=PP3V3_S5_PWRCTL 63
=PP3V3_S5_P1V05ENETFET 32
=PP3V3_S5_P3V3S3FET 64
=PP3V3_S5_P3V3S0FET 64
=PP3V3_S5_P1V05S5 62
=PP3V3_S5_MEMRESET 29
=PP3V3_S5_P3V3ENETFET 32
=PP3V3_S5_DP_PORT_PWR 67

"G3H" RAILS

55 =PP3V42_G3H_REG
PP3V42_G3H 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE
=PPVIN_S5_SMCVREF 37
=PP3V42_G3H_SMBUS_SMC_BSA 39
=PP3V42_G3H_PWRCTL 63
=PP3V42_G3H_CHGR 56
=PP3V42_G3H_SMCUSBMUX 35
=PP3V42_G3H_TPAD 44
=PP3V3_S5_SMC 36 37
=PP3V3_S5_LPCPLUS 38
=PP3V42_G3H_RTC_D 25
=PP3V42_G3H_ONEWIRE 55
=PP3V42_G3H_HALL 55

55 =PP18V5_DCIN_CONN
PP18V5_G3H
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.3 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE
=PP18V5_G3H_CHGR 56

56 =PPBUS_G3H
PPBUS_G3H 7
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPVIN_S0_MCPCORE 60
=PPVIN_S5_1V5S30V75S0 58
=PPCPUVCORE_VTT_ISNS_R 41
(BEFORE HIGH SIDE SENSING RES.)
=PPBUS_S0_LCDBKLT 69
=PPVIN_S5_3V3S5 57
=PPVIN_S3_5VS3 57
=PPBUS_G3HRS5 40

41 =PPCPUVCORE_VTT_ISNS
(AFTER HIGH SIDE CPU VCORE
& CPU VTT SENSING RES.)
PPBUS_G3H_CPU_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.3 MM
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPVIN_S0_CPUVTTS0 61
=PPVIN_S5_CPU_IMVP 59

DIGITAL GROUND
GND
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=0V

"ENET" RAILS

32 =PP3V3_ENET_FET
PP3V3_ENET_PHY 7
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_ENET_MCP_RMGT 18 23
=PP3V3_ENET_PHY 31

32 =PP1V05_ENET_FET
PP1V2R1V05_ENET 7
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_ENET_MCP_PLL_MAC 23
=PP1V05_ENET_MCP_RMGT 18 23
=PP1V05_ENET_PHY 31

PEX & SATA AVDD/DVDD aliases

23 PP1V05_S0_MCP_PEX_AVDD
MAKE_BASE=TRUE
206 mA (A01)
=PP1V05_S0_MCP_PEX_AVDD0 17
=PP1V05_S0_MCP_PEX_AVDD1 17
206 mA (A01)

23 8 =PP1V05_S0_MCP_PEX_DVDD
206 mA (A01)
=PP1V05_S0_MCP_PEX_DVDD0 17
=PP1V05_S0_MCP_PEX_DVDD1 17
57 mA (A01)

23 PP1V05_S0_MCP_SATA_AVDD
MAKE_BASE=TRUE
127 mA (A01)
=PP1V05_S0_MCP_SATA_AVDD0 20
=PP1V05_S0_MCP_SATA_AVDD1 20
127 mA (A01)

23 8 =PP1V05_S0_MCP_SATA_DVDD
127 mA (A01)
=PP1V05_S0_MCP_SATA_DVDD0 20
=PP1V05_S0_MCP_SATA_DVDD1 20
43 mA (A01)

SYNC_MASTER=K24_MLB SYNC_DATE=02/04/2009
PAGE TITLE
Power Aliases
Apple Inc.
DRAWING NUMBER 051-7982
SIZE D
REVISION C.0.0
BRANCH
PAGE 8 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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HEATSINK STANDOFFS

Z0902
STDOFF-4.50D.98H-1.1-3.48-TH
LEFT OF CPU

Z0901
STDOFF-4.50D.98H-1.1-3.48-TH
ABOVE CPU

Z0903
STDOFF-4.50D.98H-1.1-3.48-TH
BELOW MCP

Z0904
STDOFF-4.50D.98H-1.1-3.48-TH
BELOW CPU

FAN STANDOFF

OMIT
Z0905
3P2R2P7

MLB MOUNTING (TO C. BRACKET) SCREW HOLES

OMIT
Z0906
3P2R2P7

OMIT
Z0907
3P2R2P7

MLB MOUNTING (TO TOPCASE) SCREW HOLES

OMIT
Z0911
3P2R2P7

OMIT
Z0910
3P2R2P7

LVDS CONNECTOR HOLE

OMIT
Z0913
3P2R2P7

EMI IO MEDIUM POGO PINS (870-1794)

OMIT
ZS0900
2.0DIA-MED-EMI-MLB-K84
SM

OMIT
ZS0901
2.0DIA-MED-EMI-MLB-K84
SM

OMIT
ZS0902
2.0DIA-MED-EMI-MLB-K84
SM

OMIT
ZS0903
2.0DIA-MED-EMI-MLB-K84
SM

OMIT
ZS0908
2.0DIA-MED-EMI-MLB-K84
SM

OMIT
ZS0909
2.0DIA-MED-EMI-MLB-K84
SM

OMIT
ZS0911
2.0DIA-MED-EMI-MLB-K84
SM

EMI TALL POGO PINS (870-1698)

OMIT
ZS0904
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0905
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0906
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0907
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0910
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0912
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0913
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0914
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0915
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0919
2.0DIA-TALL-EMI-MLB-M97-M98
SM

EMI THINBC POGO PINS (870-1820)

OMIT
ZS0917
2.0DIA-MLB-THIN-BC-K84
SM

OMIT
ZS0918
2.0DIA-MLB-THIN-BC-K84
SM

OMIT
ZS0916
2.0DIA-MLB-THIN-BC-K84
SM

NOSTUFF
ZS0920
2.0DIA-MLB-THIN-BC-K84
SM

PCI-E ALIASES

UNUSED GPU LANES

17	=PEG_D2R_N<15:0>	NC_PEG_D2R_N<15:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
17	=PEG_D2R_P<15:0>	NC_PEG_D2R_P<15:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
17	=PEG_R2D_C_N<15:0>	NC_PEG_R2D_C_N<15:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
17	=PEG_R2D_C_P<15:0>	NC_PEG_R2D_C_P<15:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
17	PEG_PRSNT_L	TP_PEG_PRSNT_L	MAKE_BASE=TRUE
17	PEG_CLK100M_P	TP_PEG_CLK100M_P	MAKE_BASE=TRUE
17	PEG_CLK100M_N	TP_PEG_CLK100M_N	MAKE_BASE=TRUE

UNUSED EXPRESS CARD LANE

17	PCIE_EXCARD_D2R_P	TP_PCIE_EXCARD_D2R_P	MAKE_BASE=TRUE
17	PCIE_EXCARD_D2R_N	TP_PCIE_EXCARD_D2R_N	MAKE_BASE=TRUE
17	PCIE_EXCARD_R2D_C_P	TP_PCIE_EXCARD_R2D_C_P	MAKE_BASE=TRUE
17	PCIE_EXCARD_R2D_C_N	TP_PCIE_EXCARD_R2D_C_N	MAKE_BASE=TRUE
17	PCIE_EXCARD_PRSNT_L	TP_PCIE_EXCARD_PRSNT_L	MAKE_BASE=TRUE
17	EXCARD_CLKREQ_L	TP_EXCARD_CLKREQ_L	MAKE_BASE=TRUE
17	PCIE_CLK100M_EXCARD_P	TP_PCIE_CLK100M_EXCARD_P	MAKE_BASE=TRUE
17	PCIE_CLK100M_EXCARD_N	TP_PCIE_CLK100M_EXCARD_N	MAKE_BASE=TRUE

UNUSED FIREWIRE LANE

72 17	PCIE_FW_D2R_P	TP_PCIE_FW_D2R_P	MAKE_BASE=TRUE
72 17	PCIE_FW_D2R_N	TP_PCIE_FW_D2R_N	MAKE_BASE=TRUE
72 17	PCIE_FW_R2D_C_P	TP_PCIE_FW_R2D_C_P	MAKE_BASE=TRUE
72 17	PCIE_FW_R2D_C_N	TP_PCIE_FW_R2D_C_N	MAKE_BASE=TRUE
17	PCIE_FW_PRSNT_L	TP_PCIE_FW_PRSNT_L	MAKE_BASE=TRUE
17	FW_CLKREQ_L	TP_FW_CLKREQ_L	MAKE_BASE=TRUE
17	PCIE_CLK100M_FW_P	TP_PCIE_CLK100M_FW_P	MAKE_BASE=TRUE
17	PCIE_CLK100M_FW_N	TP_PCIE_CLK100M_FW_N	MAKE_BASE=TRUE

USB ALIASES

UNUSED USB PORTS

20	USB_EXTD_P	TP_USB_EXTD_P	MAKE_BASE=TRUE
20	USB_EXTD_N	TP_USB_EXTD_N	MAKE_BASE=TRUE
20	USB_EXCARD_P	TP_USB_EXCARD_P	MAKE_BASE=TRUE
20	USB_EXCARD_N	TP_USB_EXCARD_N	MAKE_BASE=TRUE
20	USB_MINI_P	TP_USB_MINI_P	MAKE_BASE=TRUE
20	USB_MINI_N	TP_USB_MINI_N	MAKE_BASE=TRUE
20	USB_EXTC_P	TP_USB_EXTC_P	MAKE_BASE=TRUE
20	USB_EXTC_N	TP_USB_EXTC_N	MAKE_BASE=TRUE
73 20	USB_CARDREADER_P	TP_USB_CARDREADER_P	MAKE_BASE=TRUE
73 20	USB_CARDREADER_N	TP_USB_CARDREADER_N	MAKE_BASE=TRUE
73 20	USB_IR_N	TP_USB_IR_N	MAKE_BASE=TRUE
73 20	USB_IR_P	TP_USB_IR_P	MAKE_BASE=TRUE

DACS ALIASES

UNUSED CRT & TV-OUT INTERFACE

18	MCP_TV_DAC_RSET	NC_MCP_TV_DAC_RSET	NO_TEST=TRUE, MAKE_BASE=TRUE
18	MCP_TV_DAC_VREF	NC_MCP_TV_DAC_VREF	NO_TEST=TRUE, MAKE_BASE=TRUE
18	MCP_CLK27M_XTALIN	NC_MCP_CLK27M_XTALIN	NO_TEST=TRUE, MAKE_BASE=TRUE
18	MCP_CLK27M_XTALOUT	NC_MCP_CLK27M_XTALOUT	NO_TEST=TRUE, MAKE_BASE=TRUE
18	CRT_IG_R_C_PR	NC_CRT_IG_R_C_PR	NO_TEST=TRUE, MAKE_BASE=TRUE
18	CRT_IG_G_Y_Y	NC_CRT_IG_G_Y_Y	NO_TEST=TRUE, MAKE_BASE=TRUE
18	CRT_IG_B_COMP_PB	NC_CRT_IG_B_COMP_PB	NO_TEST=TRUE, MAKE_BASE=TRUE
18	CRT_IG_HSYNC	NC_CRT_IG_HSYNC	NO_TEST=TRUE, MAKE_BASE=TRUE
18	CRT_IG_VSYNC	NC_CRT_IG_VSYNC	NO_TEST=TRUE, MAKE_BASE=TRUE

LVDS ALIASES

18	LVDS_IG_A_DATA_P<3>	NC_LVDS_IG_A_DATA_P3	NO_TEST=TRUE, MAKE_BASE=TRUE
18	LVDS_IG_A_DATA_N<3>	NC_LVDS_IG_A_DATA_N3	NO_TEST=TRUE, MAKE_BASE=TRUE
18	LVDS_IG_B_CLK_P	NC_LVDS_IG_B_CLK_P	NO_TEST=TRUE, MAKE_BASE=TRUE
18	LVDS_IG_B_CLK_N	NC_LVDS_IG_B_CLK_N	NO_TEST=TRUE, MAKE_BASE=TRUE
18	LVDS_IG_B_DATA_P<3:0>	NC_LVDS_IG_B_DATA_P<3:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
18	LVDS_IG_B_DATA_N<3:0>	NC_LVDS_IG_B_DATA_N<3:0>	NO_TEST=TRUE, MAKE_BASE=TRUE

MISC MCP79 ALIASES

14	CPU_PECI_MCP	TP_CPU_PECI_MCP	
19	FW_PME_L	TP_FW_PME_L	MAKE_BASE=TRUE
17	GMUX_JTAG_TCK_L	TP_GMUX_JTAG_TCK_L	MAKE_BASE=TRUE
17	GMUX_JTAG_TDO	TP_GMUX_JTAG_TDO	MAKE_BASE=TRUE
19	GMUX_JTAG_TDI	TP_GMUX_JTAG_TDI	MAKE_BASE=TRUE
19	GMUX_JTAG_TMS	TP_GMUX_JTAG_TMS	MAKE_BASE=TRUE
21	MCP_GPIO_4	MIKEY_MIC_LOAD_DET	MAKE_BASE=TRUE, 54
17	CARDREADER_RESET	TP_CARDREADER_RESET	MAKE_BASE=TRUE

LAN ALIASES

18	=MCP_MII_RXER	MCP_MII_PD	MAKE_BASE=TRUE
18	=MCP_MII_COL		
18	=MCP_MII_CRS		

R0930
47K
5%
1/16W
MF-LF
402

DP HOTPLUG PULL-DOWN

18	=DVI_HPD_GMUX_INT	HPLUG_DET2	MAKE_BASE=TRUE

R0940
20K
5%
1/16W
MF-LF
402

SO-DIMM ALIASES

UNUSED ADDRESS PINS

27	MEM_A_A<15>	TP_MEM_A_A15	MAKE_BASE=TRUE
28	MEM_B_A<15>	TP_MEM_B_A15	MAKE_BASE=TRUE

ETHERNET ALIASES

32	=P3V3ENET_EN	PM_SLP_RMGT_L 21	MAKE_BASE=TRUE
32	=P1V05ENET_EN		
31	=PP3V3_ENET_PHY_VDDREG	RTL8211_VDDREG	MAKE_BASE=TRUE
31	=RTL8211_REGOUT	NC_RTL8211_REGOUT	MAKE_BASE=TRUE
31	=RTL8211_ENSWREG		
31	TP_RTL8211_CLK125	RTL8211_CLK125	MAKE_BASE=TRUE

R0931
22
5%
1/10W
MF-LF
402

CPU FSB FREQUENCY STRAPS

70 18 IN CPU_BSEL<0:2> MAKE_BASE=TRUE — =MCP_BSEL<0:2> OUT 14

BSEL<2..0>	FSB MHZ
0 0 0	266
0 0 1	133
0 1 0	200
0 1 1	(166)
1 0 0	333
1 0 1	100
1 1 0	(400)
1 1 1	(RSVD)

SMC ALIASES

36	SMC_SYS_KBDLED	TP_SMC_SYS_KBDLED MAKE_BASE=TRUE

CPU VCORE ALIASES

59	IMVP6_VR_TT	TP_IMVP6_VR_TT MAKE_BASE=TRUE
59	IMVP6_NTC	TP_IMVP6_NTC MAKE_BASE=TRUE

SYNC MASTER=K24 MLB SYNC DATE=02/04/2009

PAGE TITLE
SIGNAL ALIAS

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D
REVISION C.0.0
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PAGE 9 OF 109
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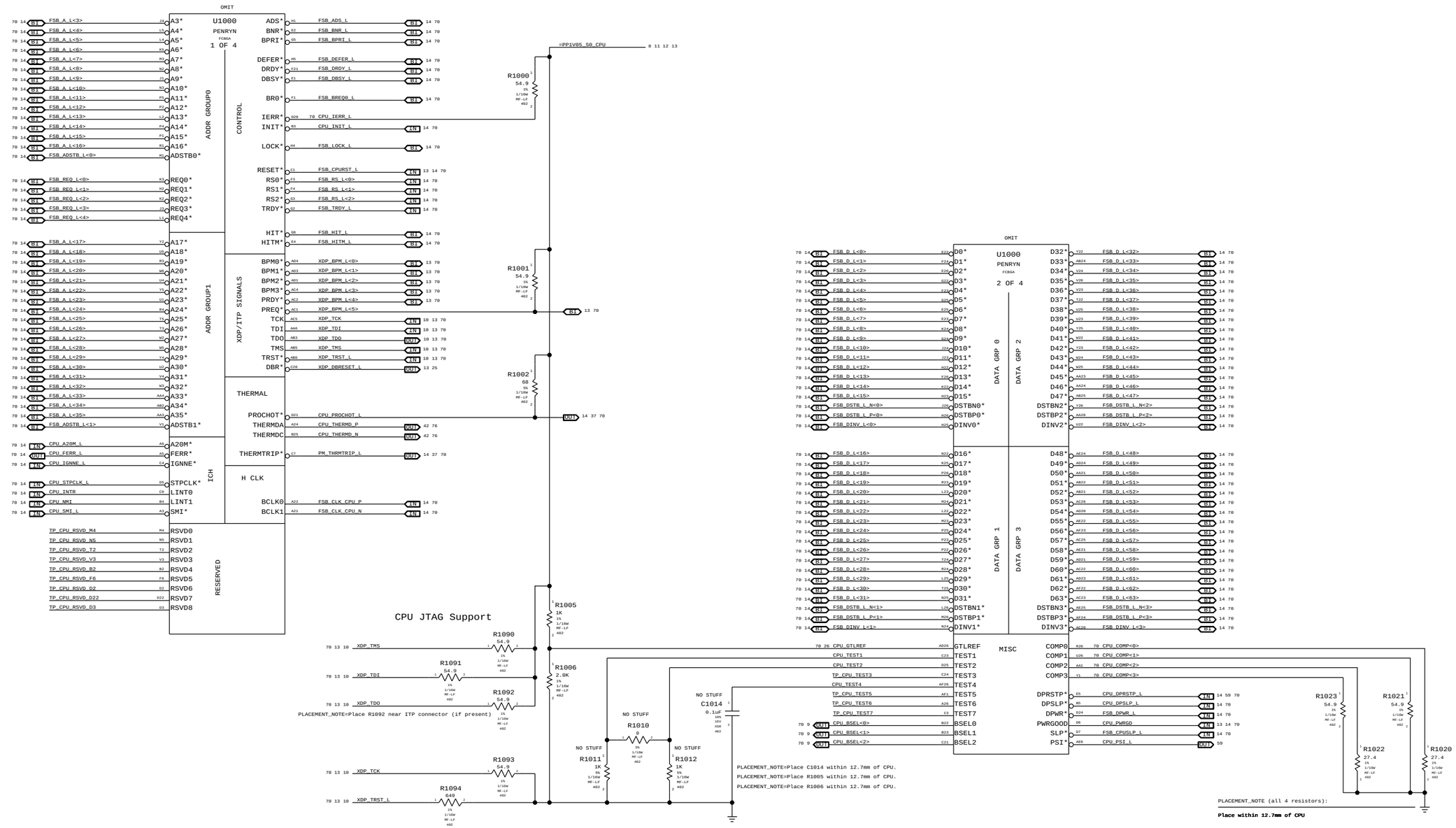

SYNC FROM T18

CHANGE CPU FROM SOCKET TO BGA SYMBOL

SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

PAGE TITLE

CPU FSB

Apple Inc.

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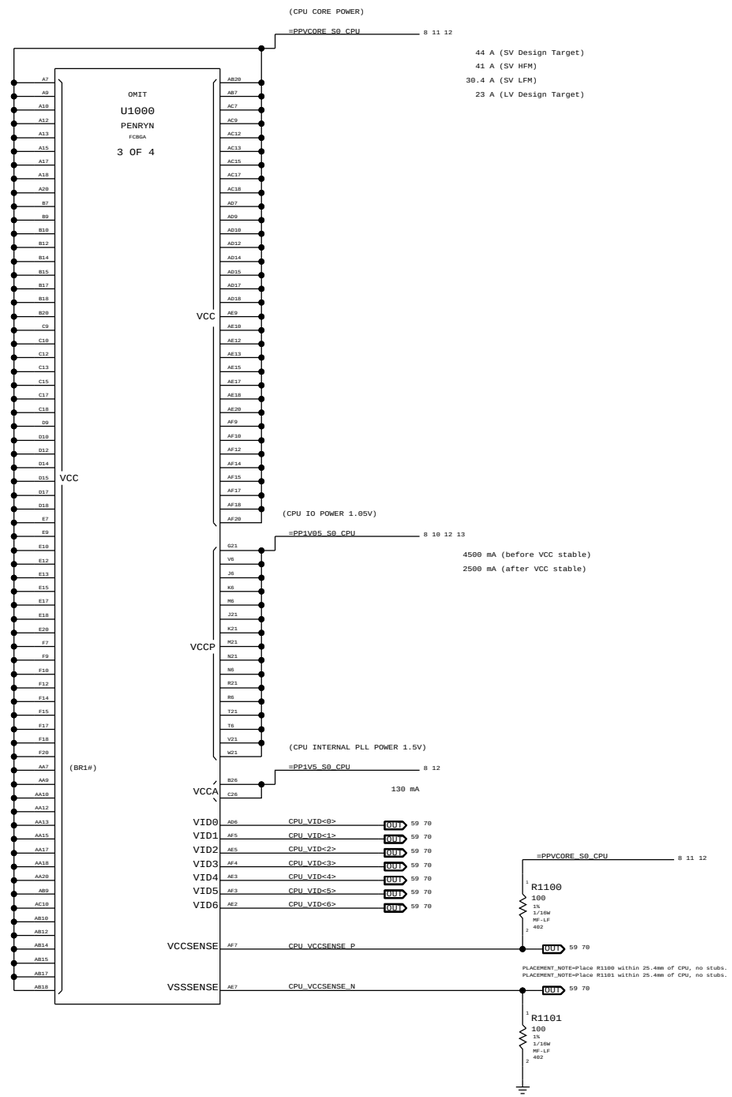

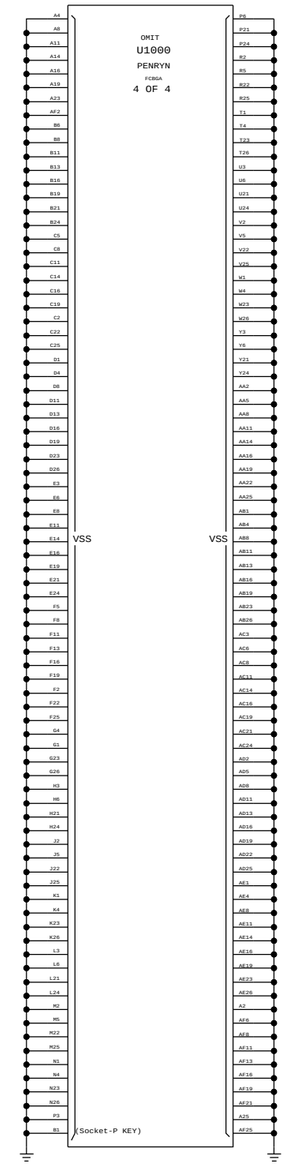

SYNC FROM T18

CHANGE CPU FROM SOCKET TO BGA SYMBOL

Current numbers from Merom for Santa Rosa EMTS, doc #20905.

SYNC MASTER=K24 MLB SYNC DATE=04/06/2006

PAGE TITLE: CPU Power & Ground

Apple Inc.

DRAWING NUMBER: 051-7982 SIZE: D

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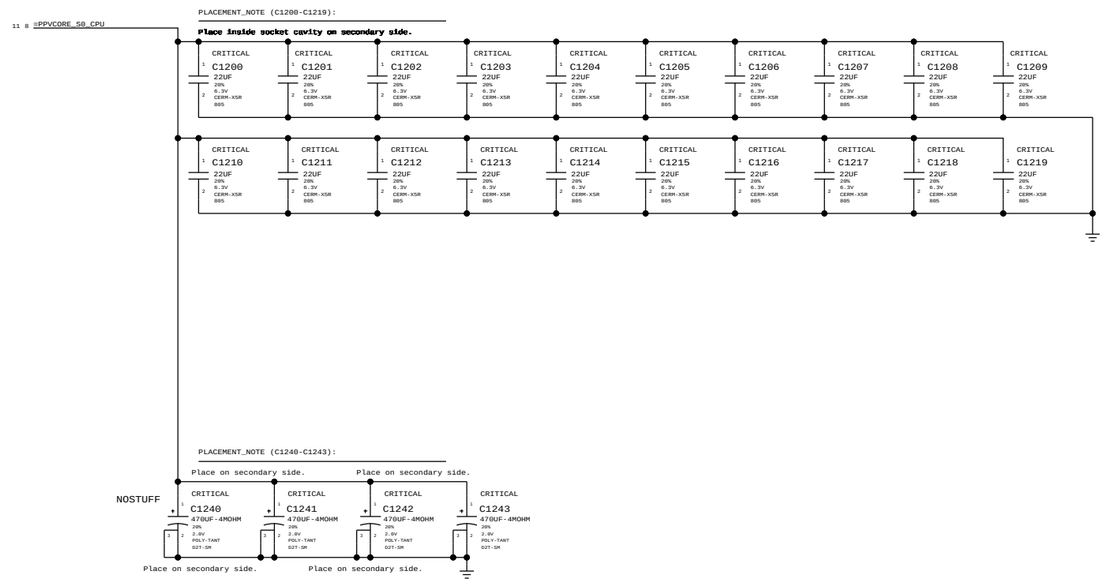
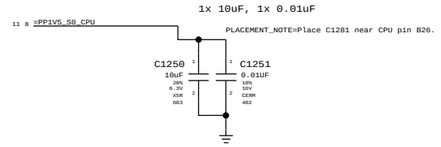
CPU VCore HF and Bulk Decoupling

4X 330UF. 20X 22UF 0805



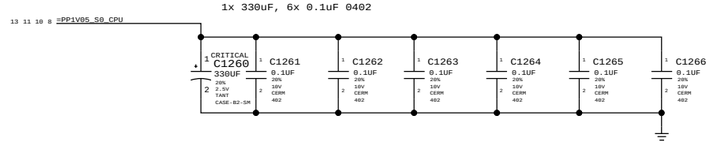
VCCA (CPU AVdd) DECOUPLING

1x 10uF, 1x 0.01uF



VCCP (CPU I/O) DECOUPLING

1x 330uF, 6x 0.1uF 0402



SYNC FROM T18
REMOVE NO STUFF CAPS C1220 TO C1231
REMOVE C1244 & C1245
CHANGE C1240-C1243 AND C1260 FROM 128S0241(9 MILLI-OHM) TO 128S0231(6 MILLI-OHM)

SYNC MASTER=K24 MLB SYNC DATE=03/30/2009

PAGE TITLE: CPU Decoupling

Apple Inc.

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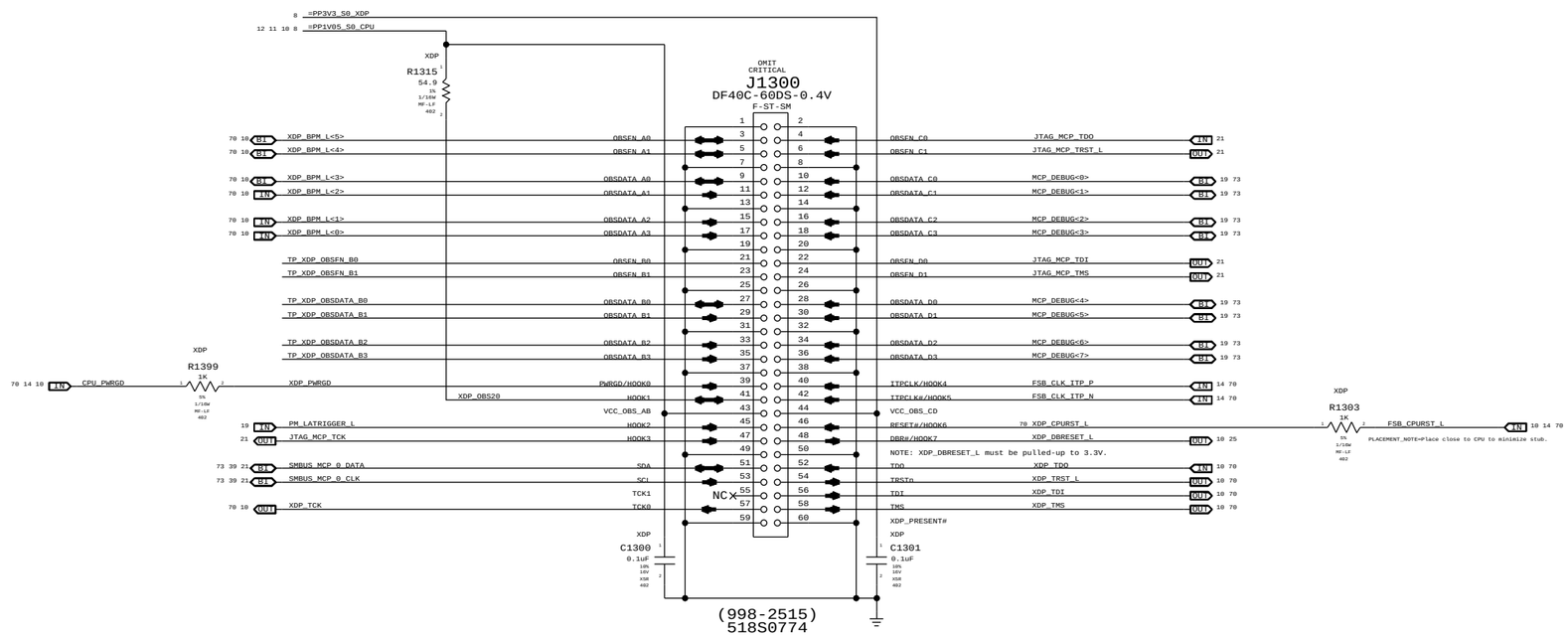
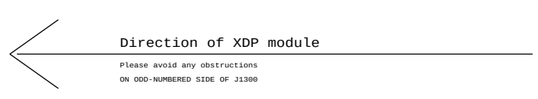
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

USE WITH 920-0782 ADAPTER FLEX TO SUPPORT CPU, MCP DEBUGGING.

MCP79-specific pinout





SYNC_MASTER=K24_MLB SYNC_DATE=02/25/2009

PAGE TITLE

eXtended Debug Port(MiniXDP)

Apple Inc.

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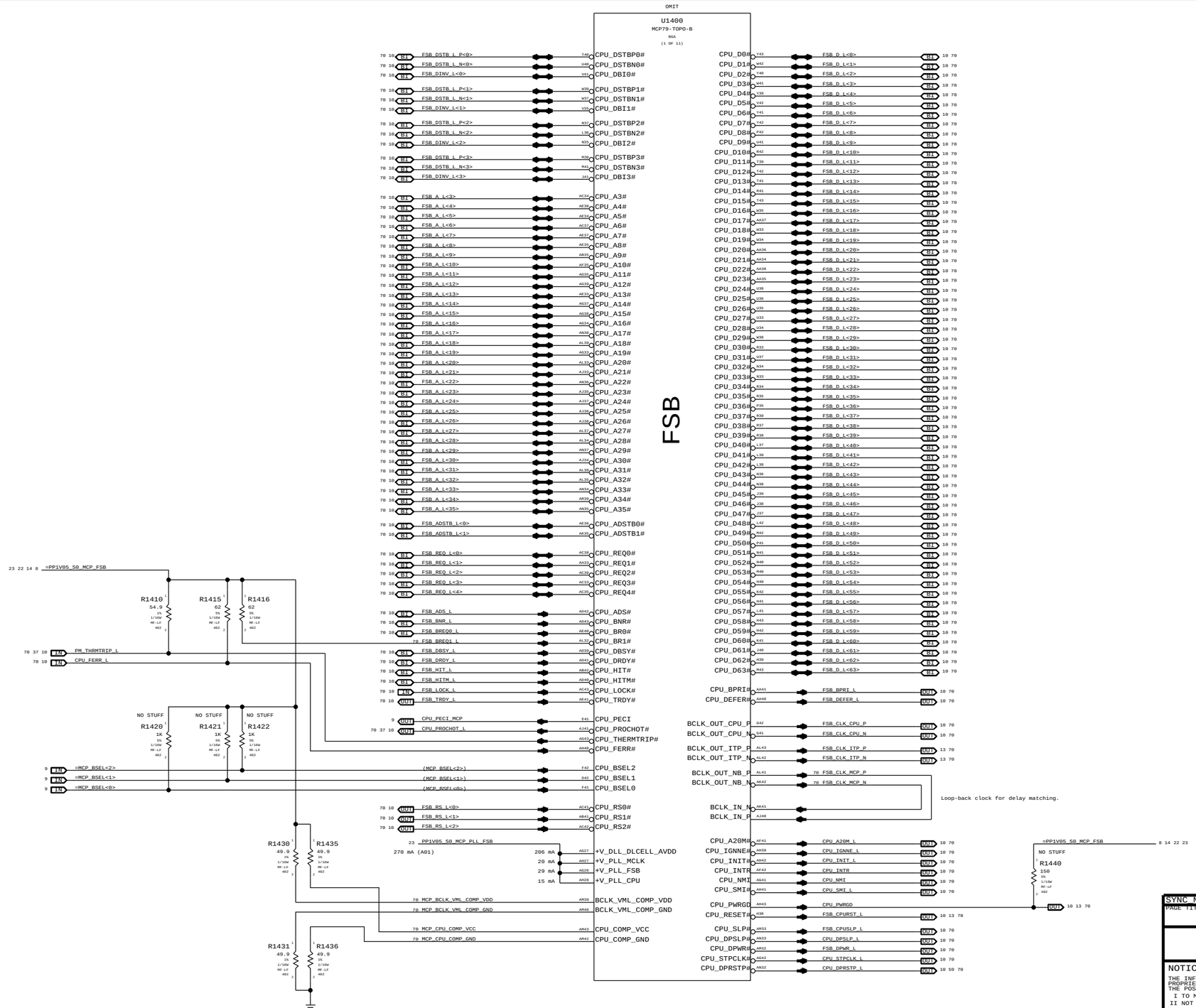

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

PAGE TITLE

MCP CPU Interface

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

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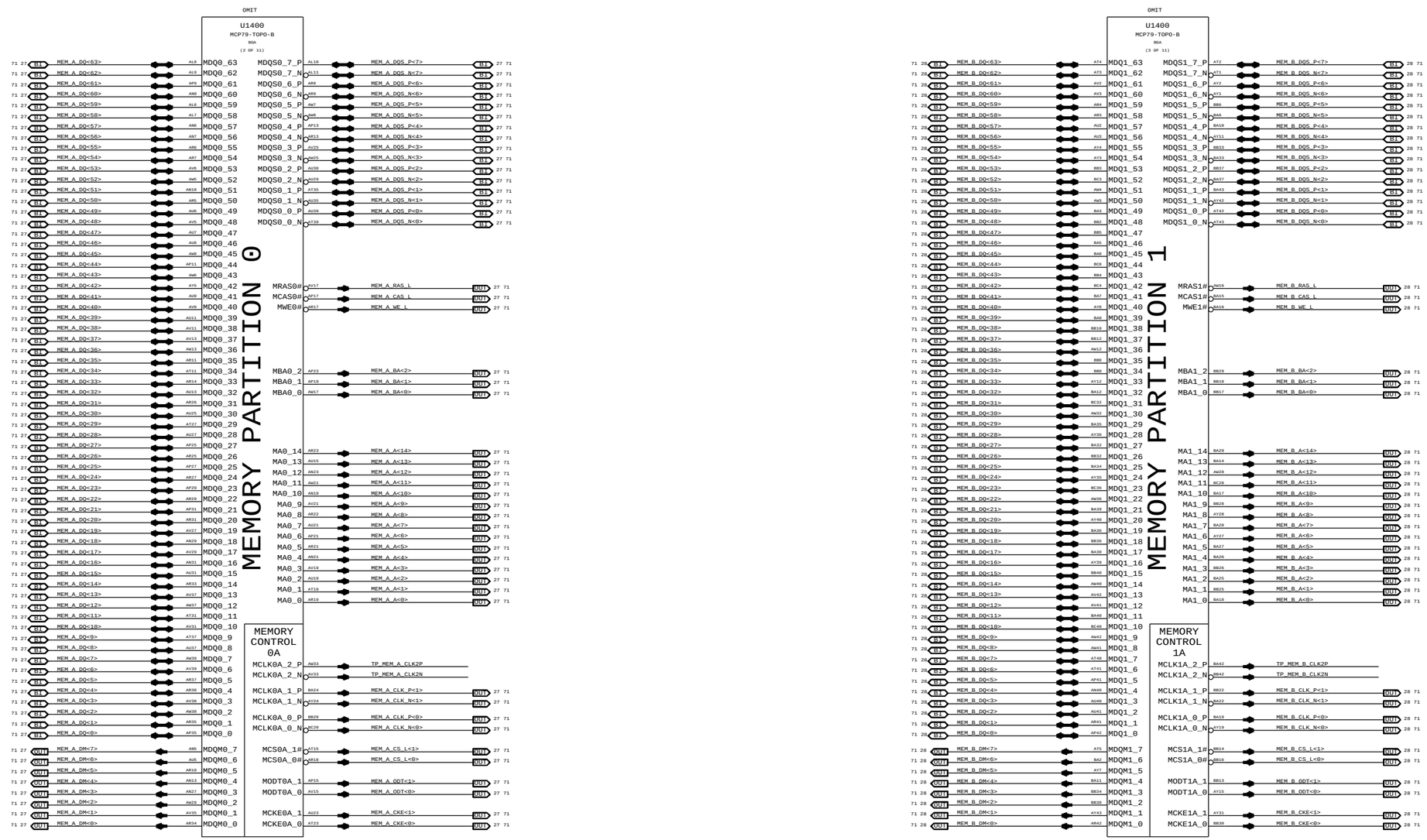

SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

PAGE TITLE
MCP Memory Interface

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

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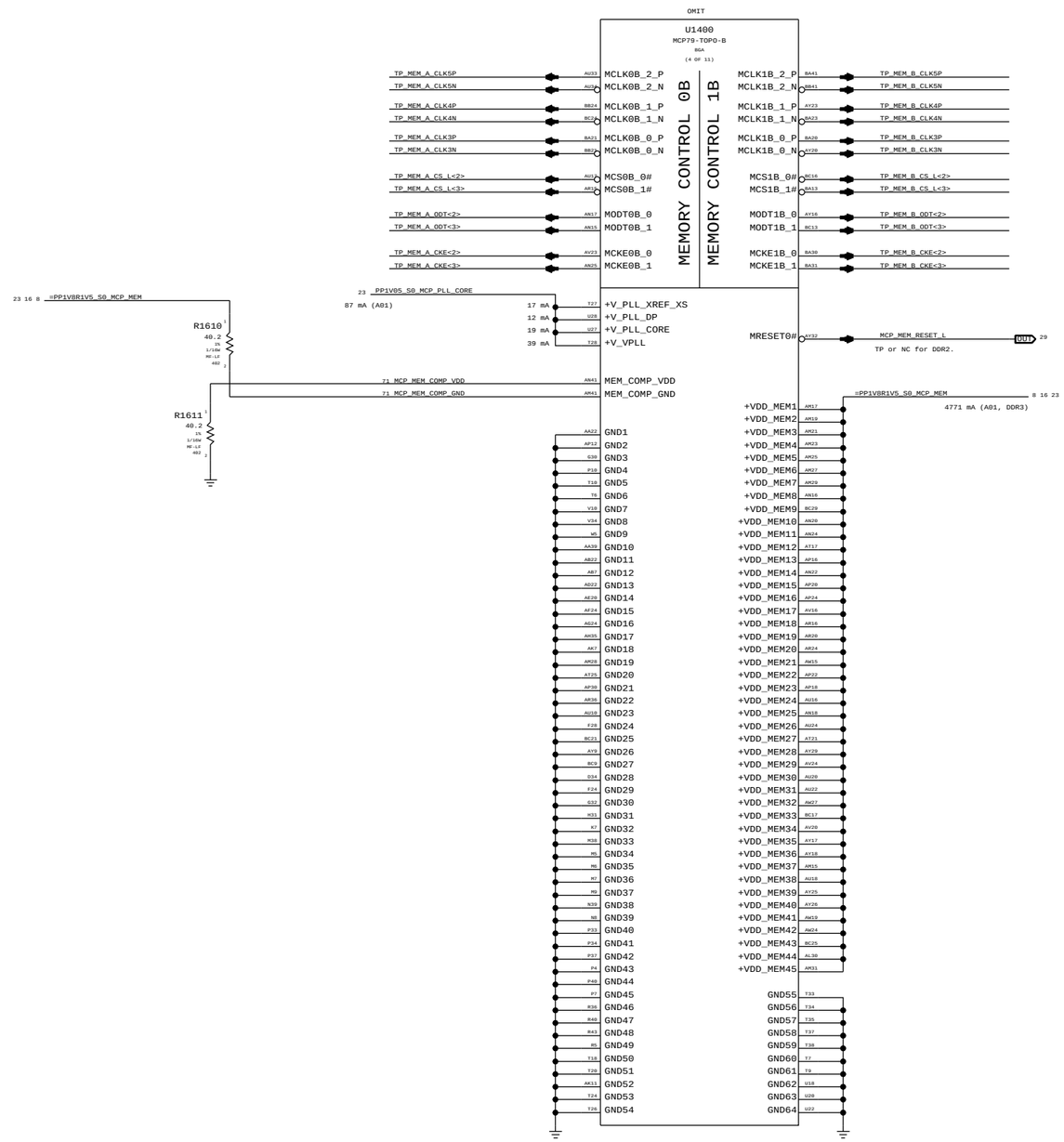

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PAGE TITLE
MCP Memory Misc

Apple Inc.

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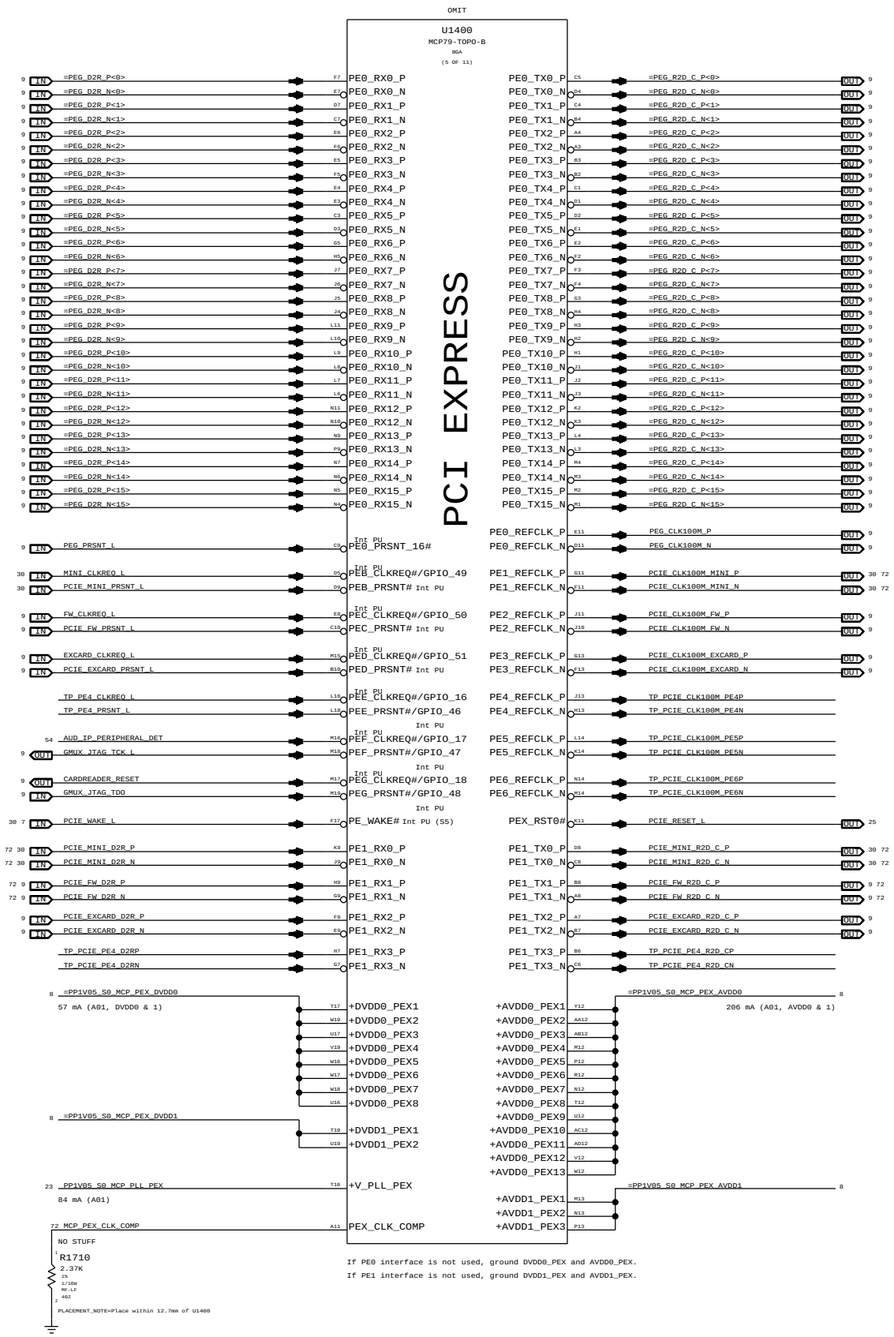

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SYNC_MASTER=K24_MLB SYNC_DATE=04/06/2009

PAGE TITLE
MCP PCIe Interfaces

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

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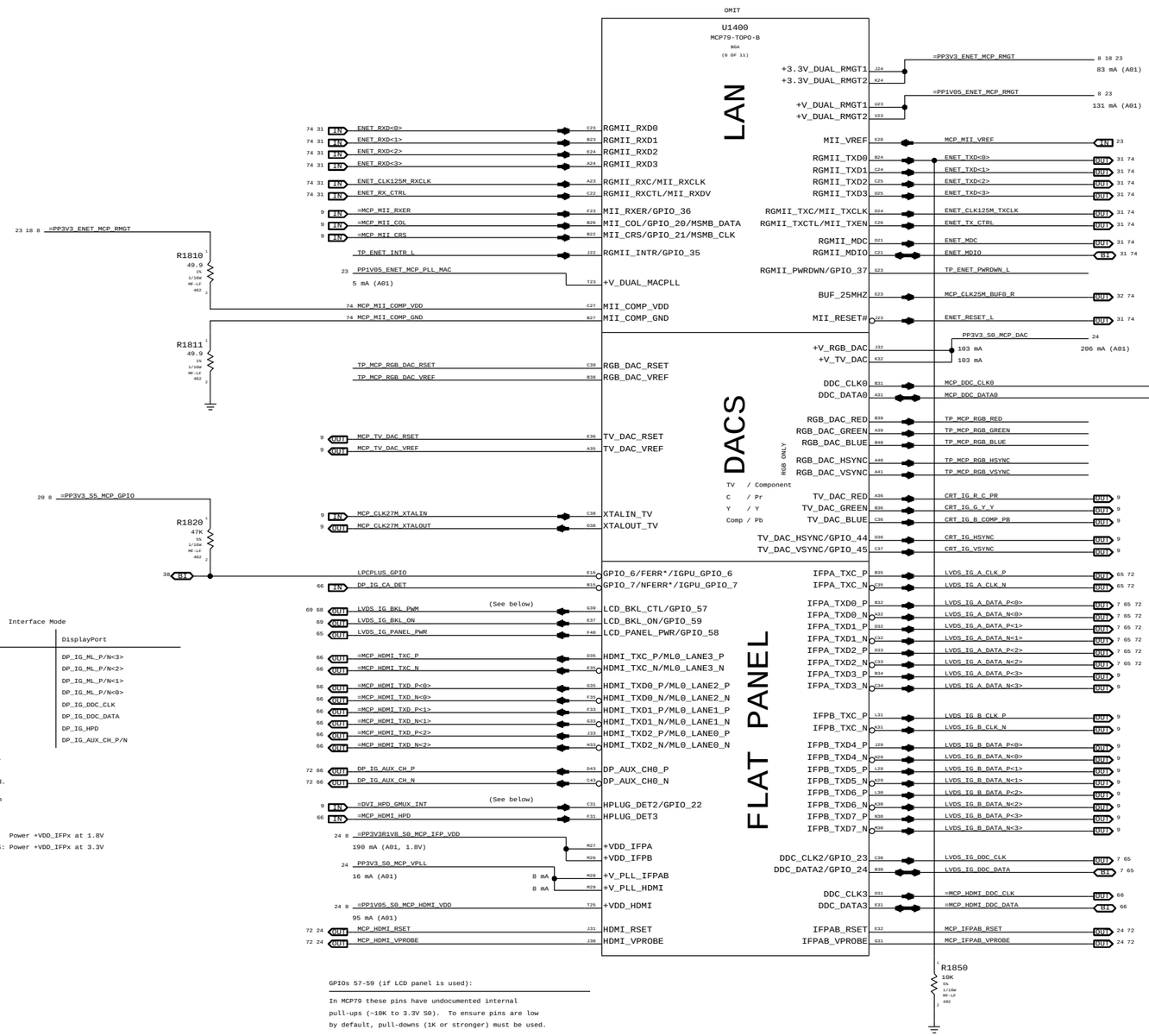

Interface Mode

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CHP/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.

NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:

Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

GPIOs 57-59 (if LCD panel is used):

In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:

Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

PAGE TITLE
MCP Ethernet & Graphics

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D
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PAGE 18 OF 109
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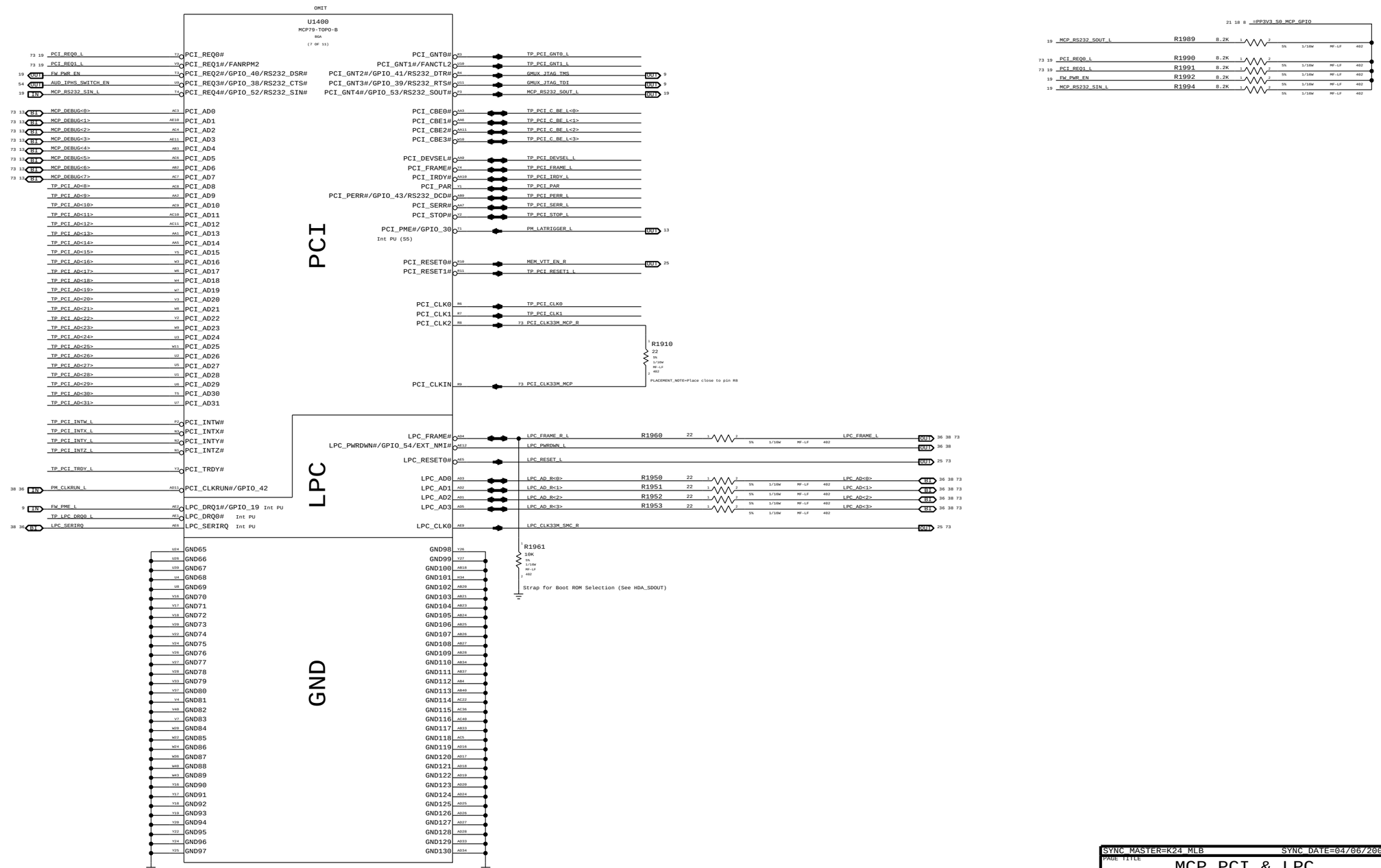

SYNC MASTER=K24 MLB	SYNC DATE=04/06/2009
PAGE TITLE	MCP PCI & LPC
Apple Inc.	DRAWING NUMBER 051-7982 SIZE D
	REVISION C.0.0
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	PAGE 19 OF 109
	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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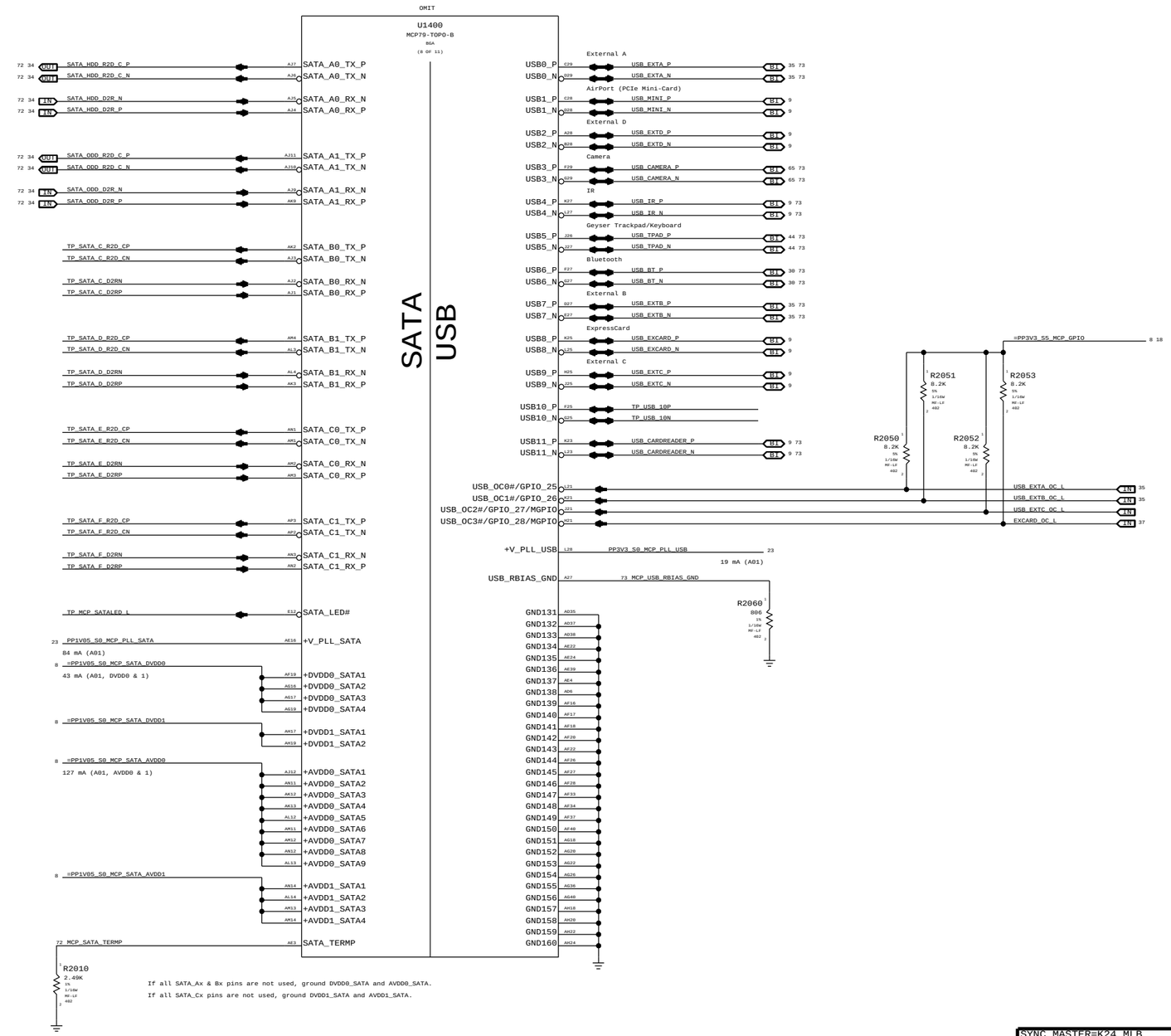

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SYNC_MASTER=K24_MLB SYNC_DATE=04/06/2009

PAGE TITLE
MCP SATA & USB

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

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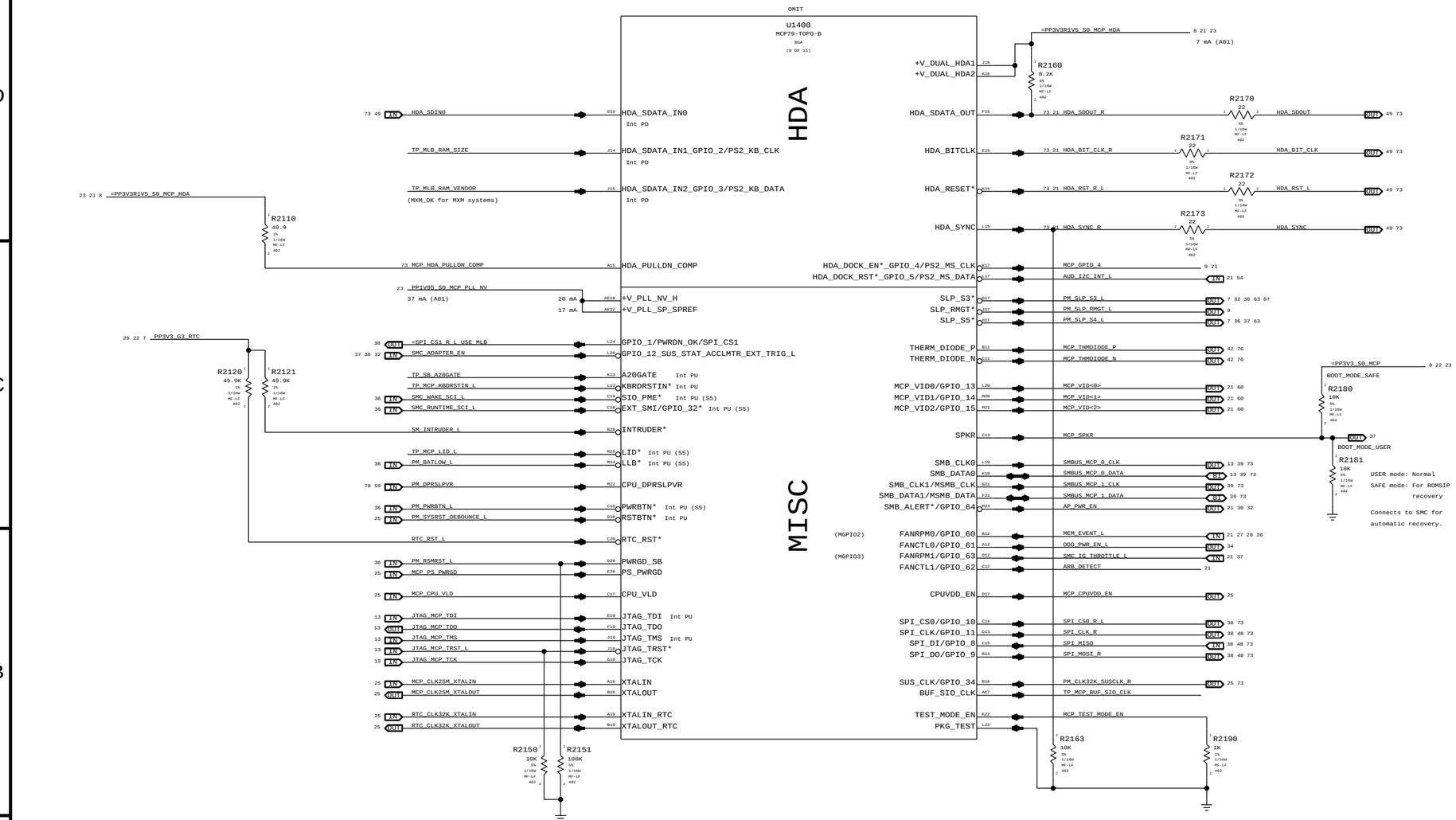


BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

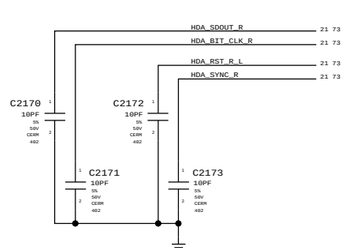
SPI Frequency Select

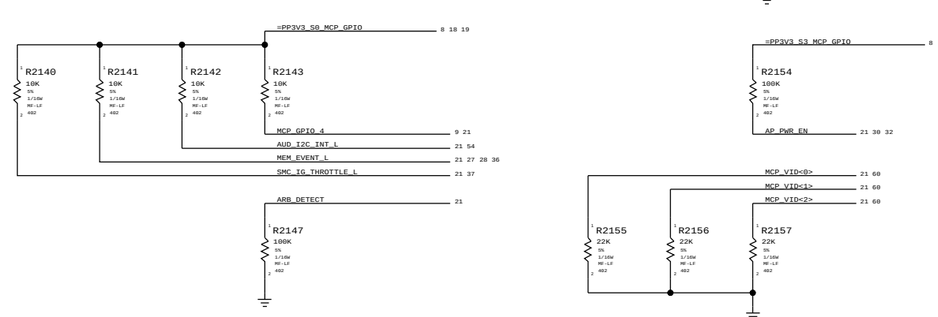
Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

HDA Output Caps

For EMI Reduction on HDA interface





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SYNC MASTER=K24 MLB SYNC DATE=03/24/2009

PAGE TITLE

MCP HDA & MISC

Apple Inc.

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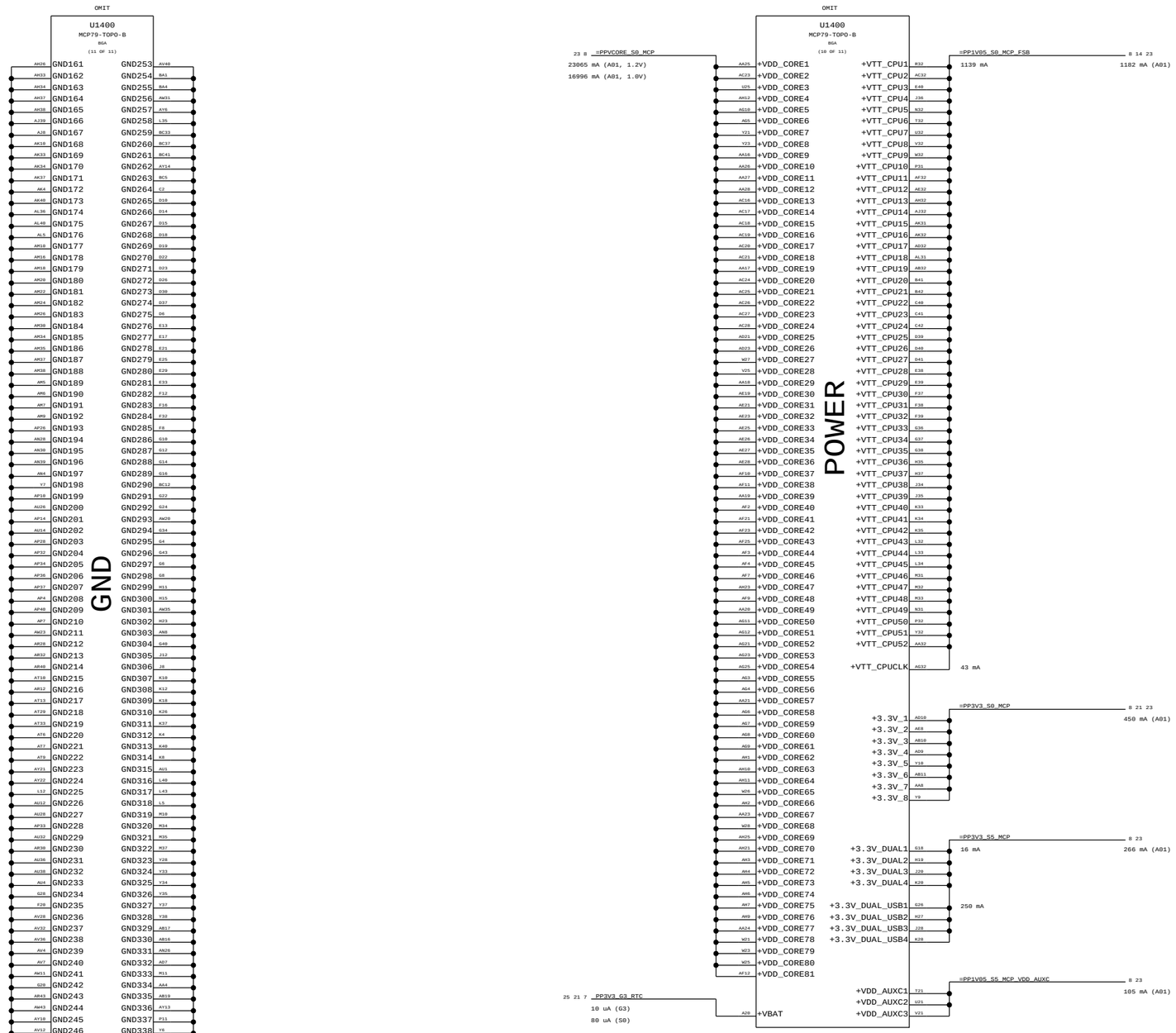

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC_MASTER=K24_MLB SYNC_DATE=04/06/2009

PAGE TITLE
MCP Power & Ground

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

REVISION C.0.0

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PAGE 22 OF 109

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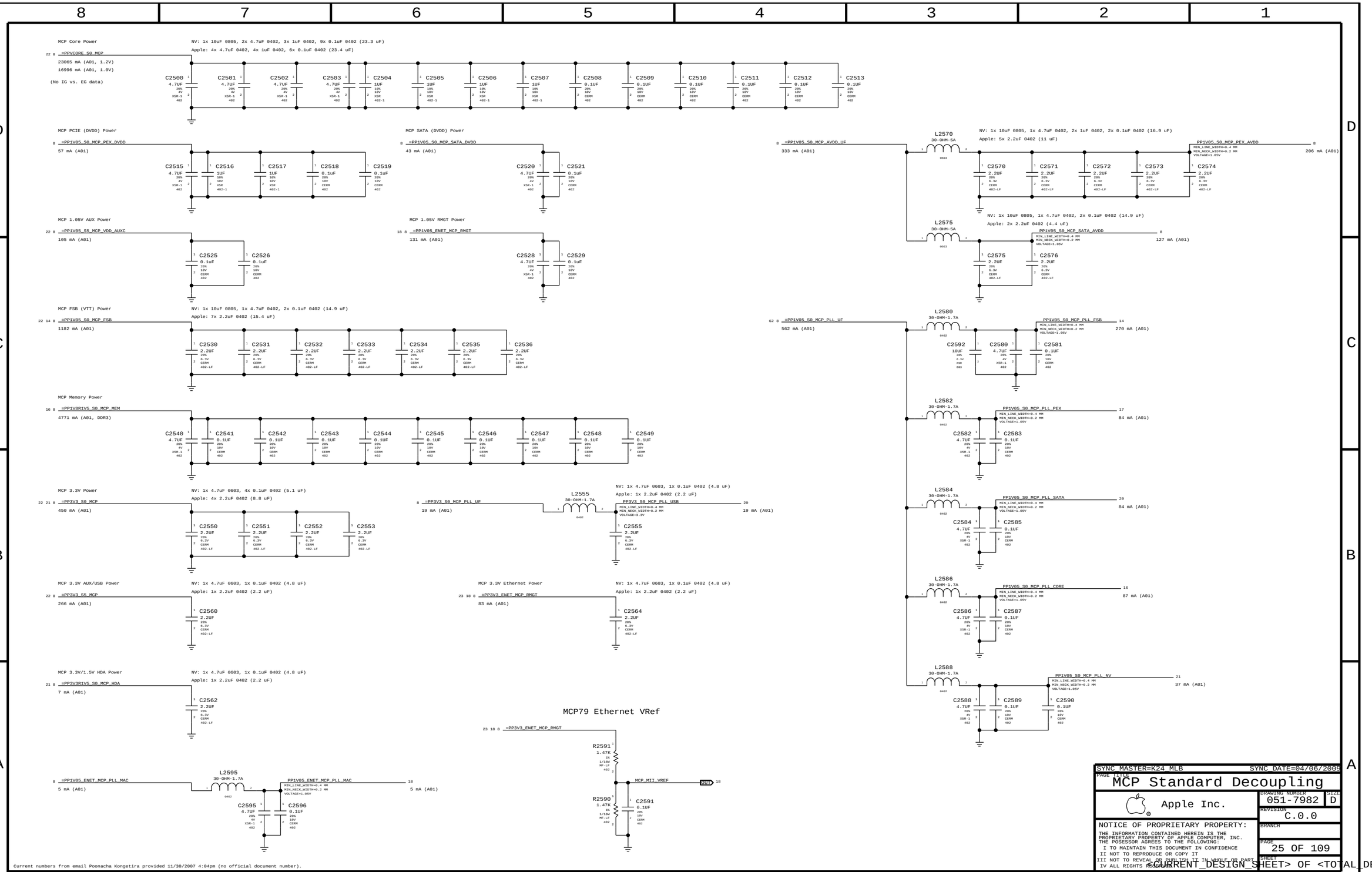

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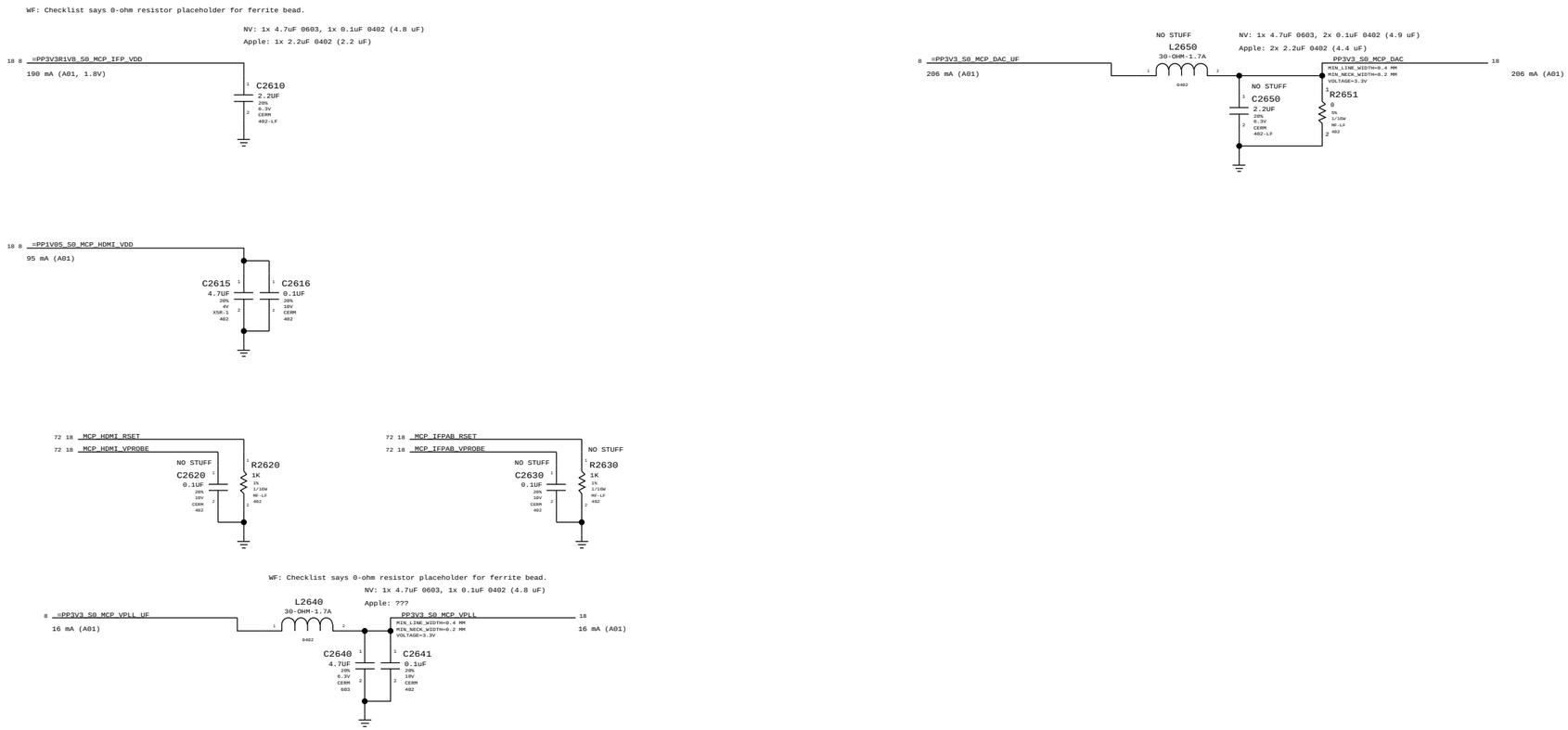

SYNC FROM T18
REMOVE MCP 27MHZ CRYSTAL CRICUIT SINCE NOT SUPPORTING TV-OUT
REMOVE DAC TERMINATIONS R2665,C2665 AND R2670 TO R2672
NOSTUFF PP3V3_S0_MCP_DAC RAIL COMPONENTS (L2650 AND C2650)
CHANGE C2651 TO R2651 TO GND PP3V3_S0_MCP_DAC
REMOVE HDCP ROMS

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC_MASTER=K24_MLB SYNC_DATE=04/06/2009

PAGE TITLE
MCP Graphics Support

Apple Inc.

DRAWING NUMBER 051-7982
SIZE D
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PAGE 26 OF 109
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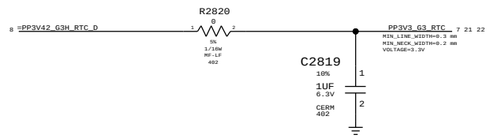
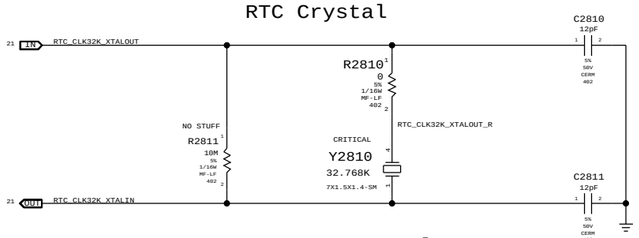


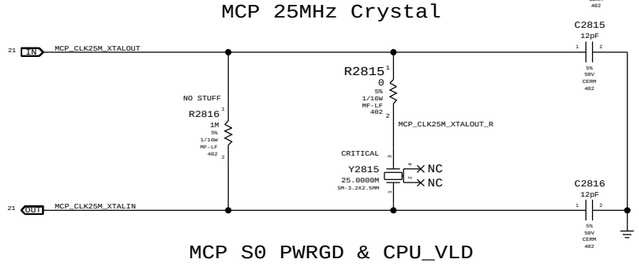
PLACEMENT_NOTE=PLACE C2819 CLOSE TO MCP79

PLACE C2819 CLOSE TO MCP79

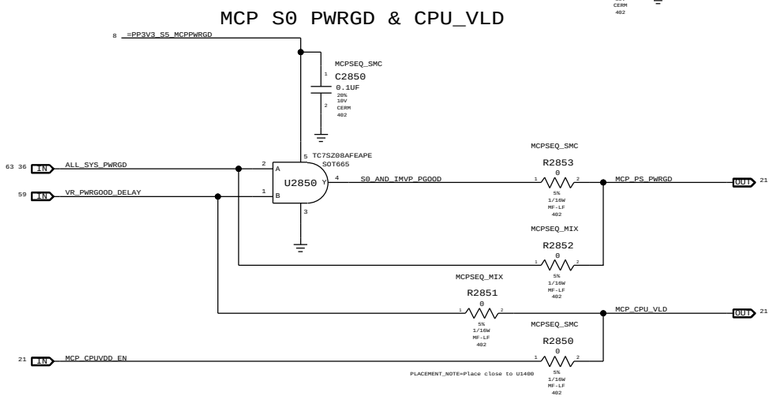
RTC Crystal



MCP 25MHz Crystal



MCP S0 PWRGD & CPU_VLD



MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up.

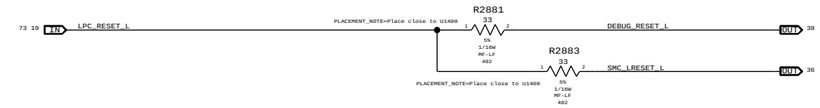
MCPSEQ_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP FSB I/O interface initialization.

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

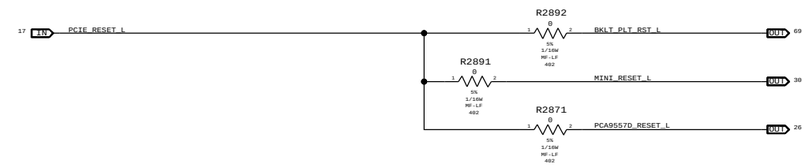
NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

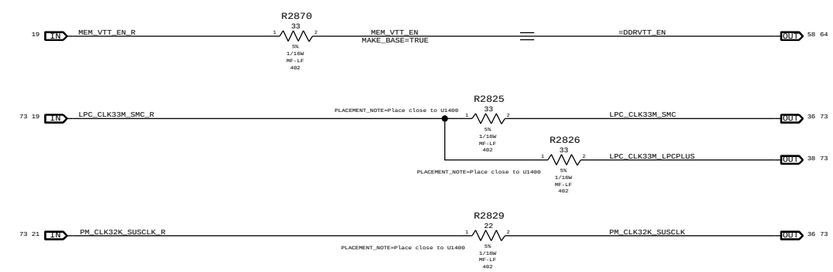
Platform Reset Connections

LPC Reset (Unbuffered)

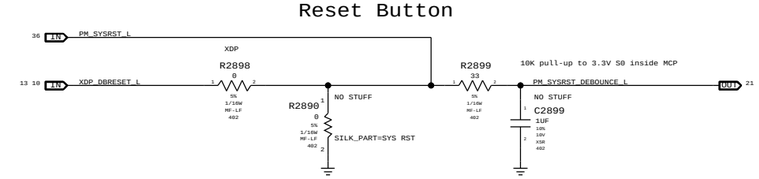


PCIE Reset (Unbuffered)





Reset Button



SYNC FROM T18
CHANGE RESET BUTTOM TO RESET PADS
REMOVE UNUSED PCIE RESET SIGNALS
REMOVE R2824 AND NET PCI_CLK33M_SLOT_A
CHANGE RTC COIN CELL TO LDO & SUPERCAP
ALIAS MEM_VTT_EN TO =DDRVTT_EN
CHANGE Y2810 AND U2850 TO SMALLER PARTS

SYNC_MASTER=K24_MLB	SYNC_DATE=02/15/2008
PAGE TITLE: SB Misc	
Apple Inc.	DRAWING NUMBER: 051-7982 SIZE: D
	REVISION: C.0.0
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	PAGE: 28 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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Page Notes

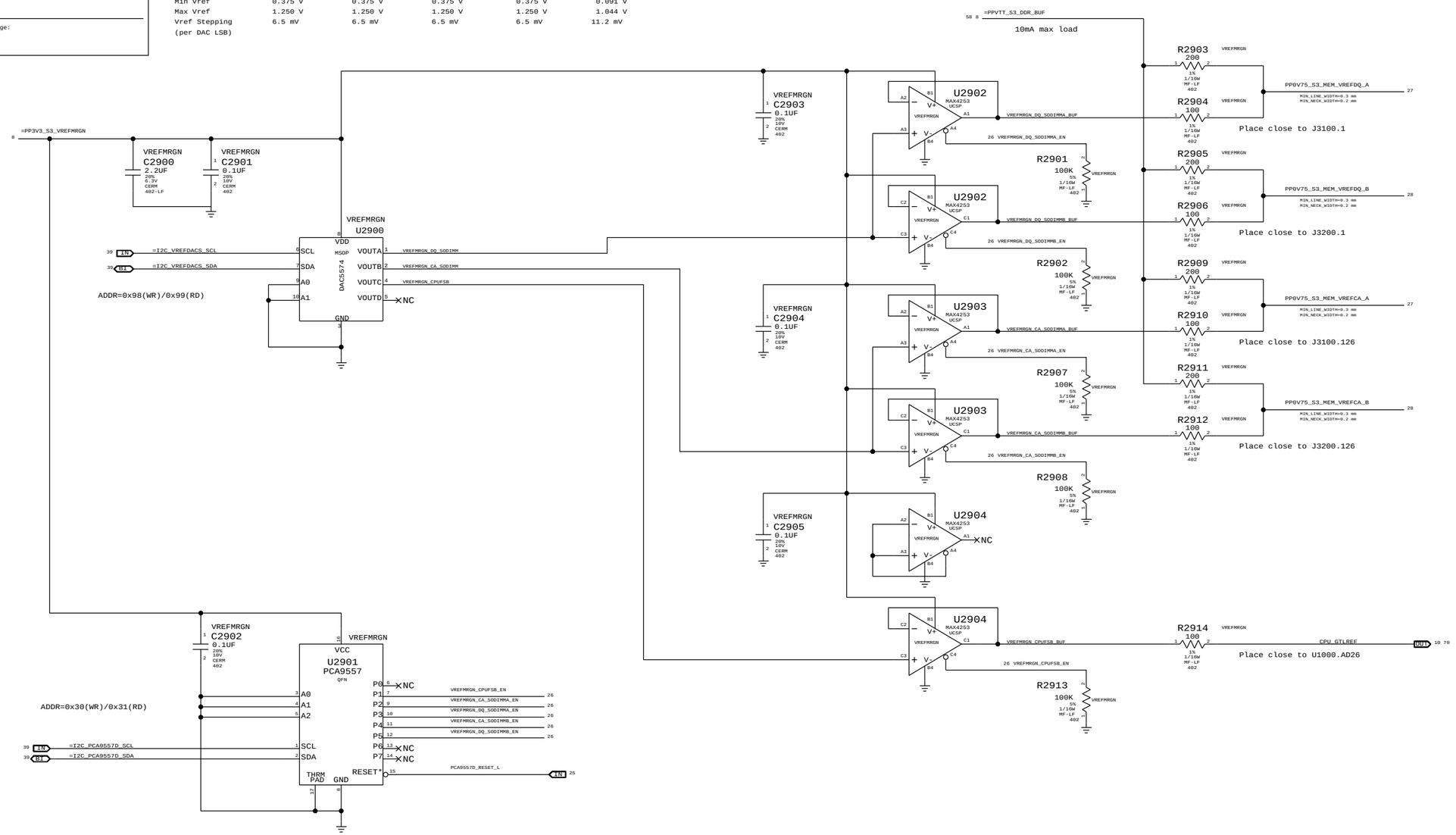
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
NO_VREFMRGN

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF
DAC channel	A	B	A	B	C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

SYNC_MASTER=K24_MLB SYNC_DATE=04/06/2009

PAGE TITLE
FSB/DDR3 Vref Margining

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D
REVISION C.0.0
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PAGE 29 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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Page Notes

Power aliases required by this page:

- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

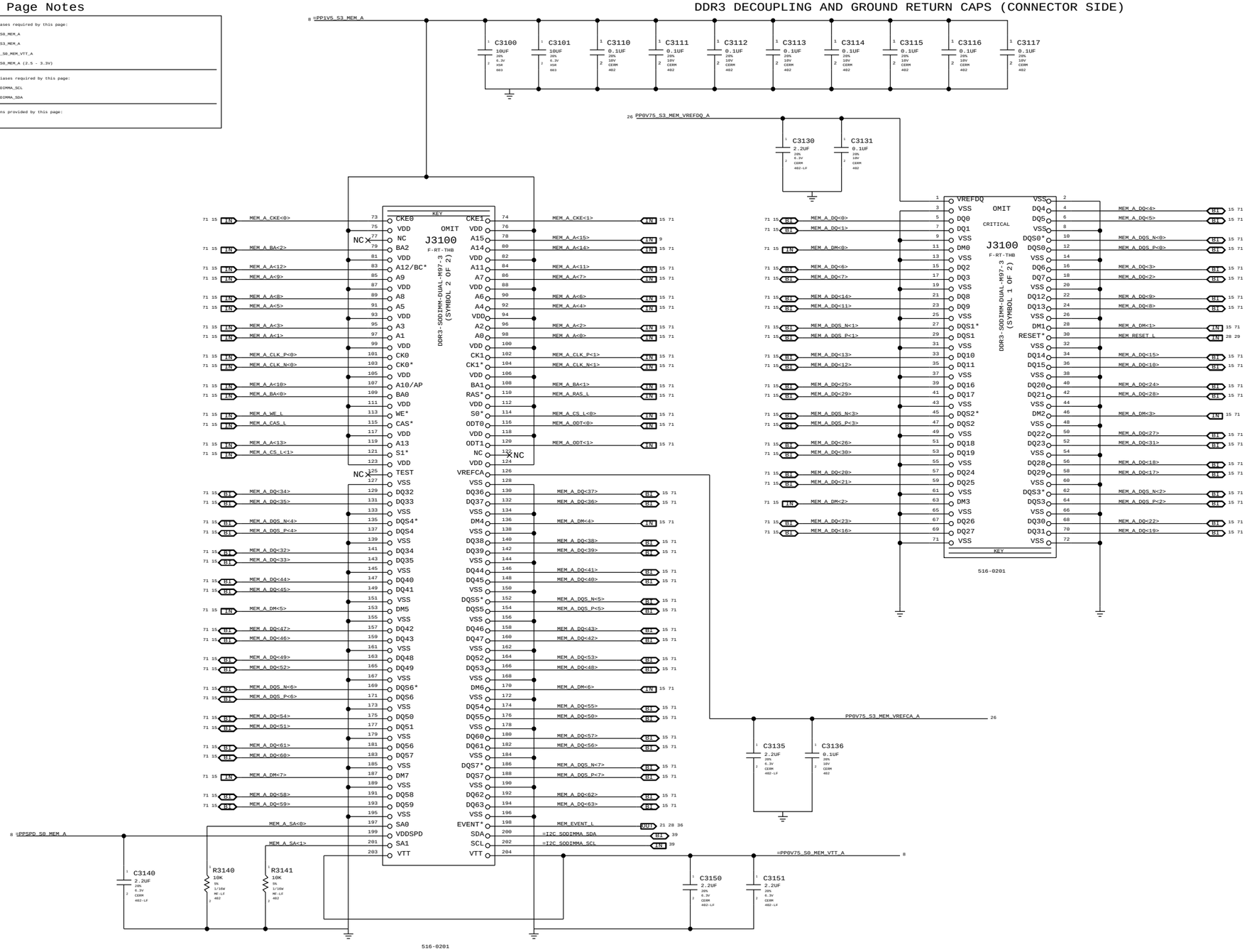
Signal aliases required by this page:

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:

(NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)



"Factory" (top) slot

SYNC MASTER=K24 MLB SYNC DATE=02/05/2009

PAGE TITLE
DDR3 SO-DIMM Connector A

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

REVISION C.0.0

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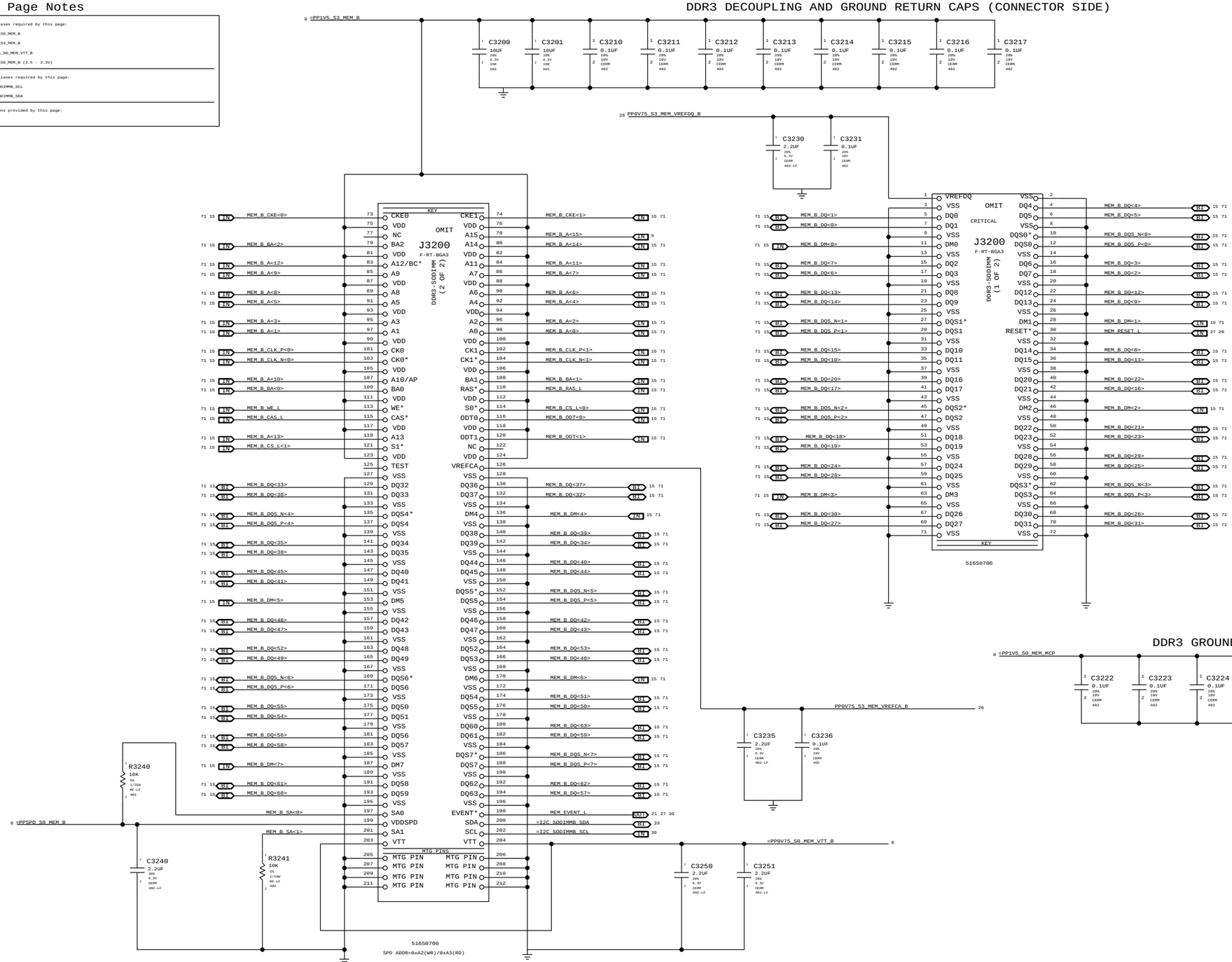
Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

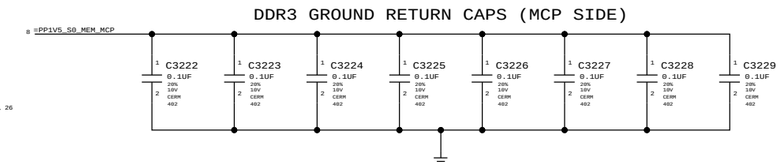
Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)



DDR3 GROUND RETURN CAPS (MCP SIDE)



"Expansion" (bottom) slot

SYNC MASTER=K24 MLB SYNC DATE=02/05/2009

PAGE TITLE
DDR3 SO-DIMM Connector B

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D
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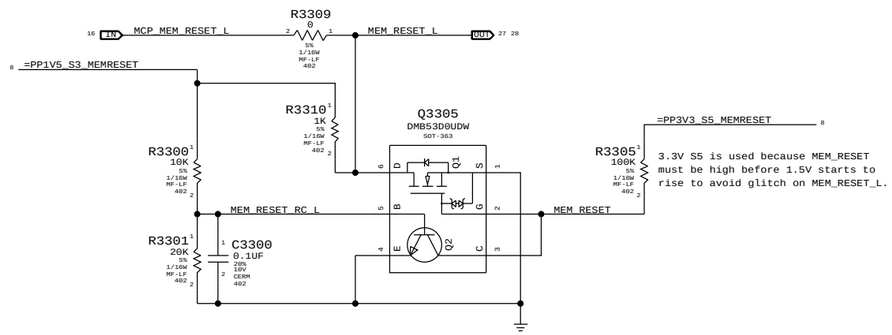
DDR3 RESET Support

Required becaues MCP79 does not meet DDR3 spec power-up reset timing requirement.



SYNC_MASTER=K24_MLB SYNC_DATE=04/06/2009

PAGE TITLE
DDR3 Support

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

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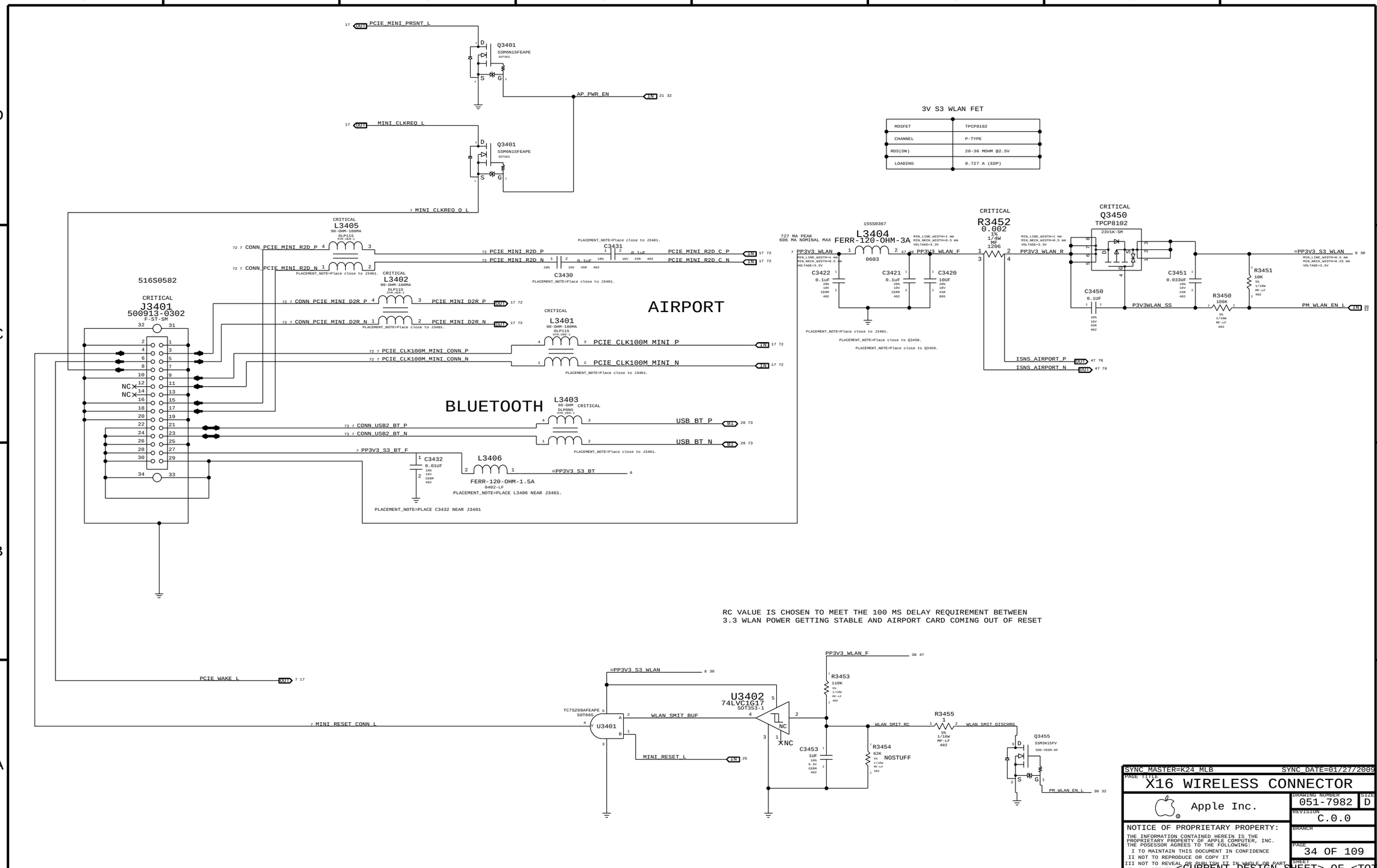

SYNC MASTER=K24_MLB SYNC DATE=01/27/2009

PAGE TITLE

X16 WIRELESS CONNECTOR

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

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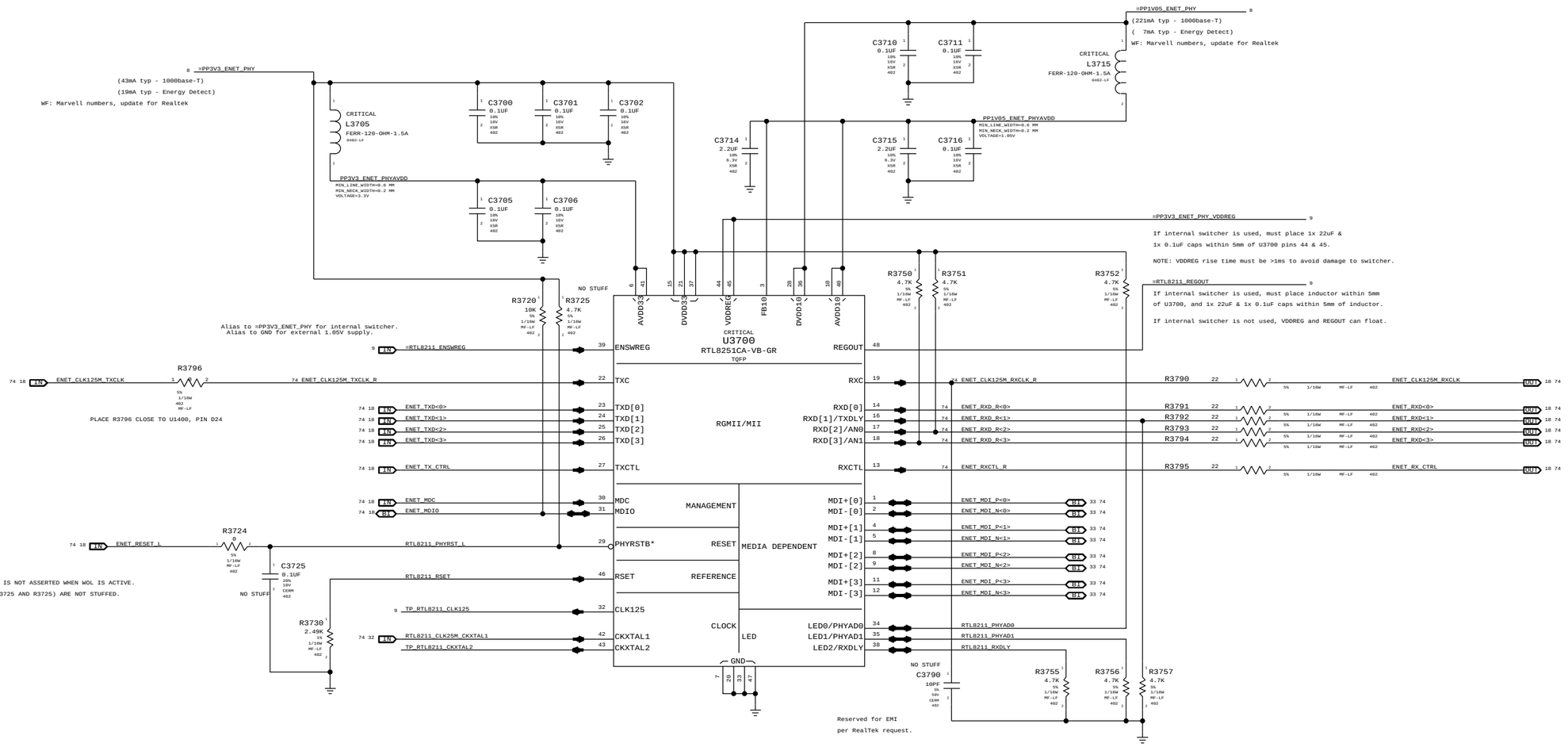

Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

PAGE TITLE
Ethernet PHY (RTL8211CL)

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D
REVISION C.0.0
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SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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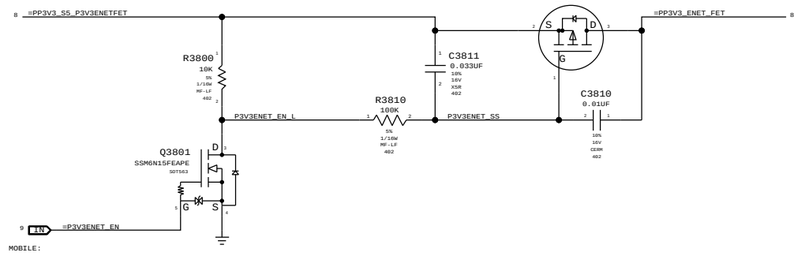
3.3V ENET FET

@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)

CRITICAL



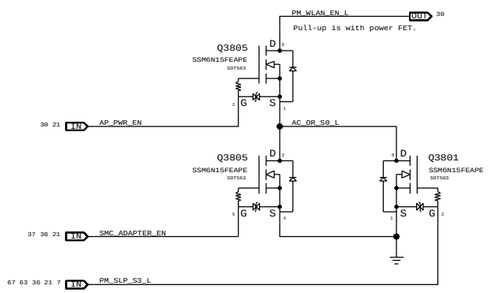
MOBILE:

Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

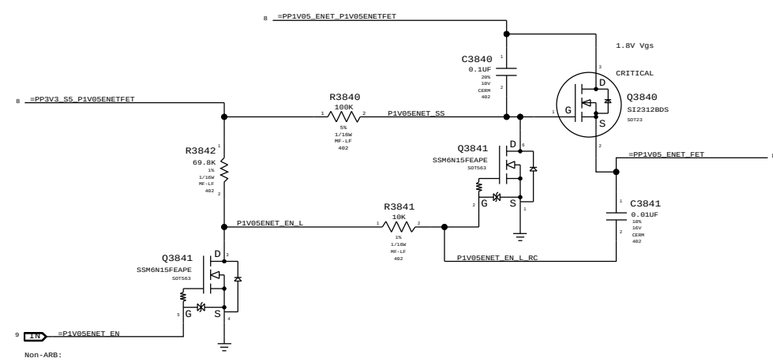
WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



1.05V ENET FET

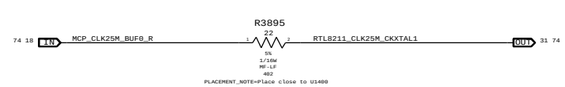


Non-ARB:

Recommend aliasing PM_SLP_RMGT_L and =P1V05ENET_EN. Nets separated on ARB for alternate power options.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



SYNC MASTER=K24 MLB	SYNC DATE=04/06/2009
PAGE TITLE: Ethernet & AirPort Support	
Apple Inc.	DRAWING NUMBER: 051-7982 SIZE: D
	REVISION: C.0.0
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	PAGE: 38 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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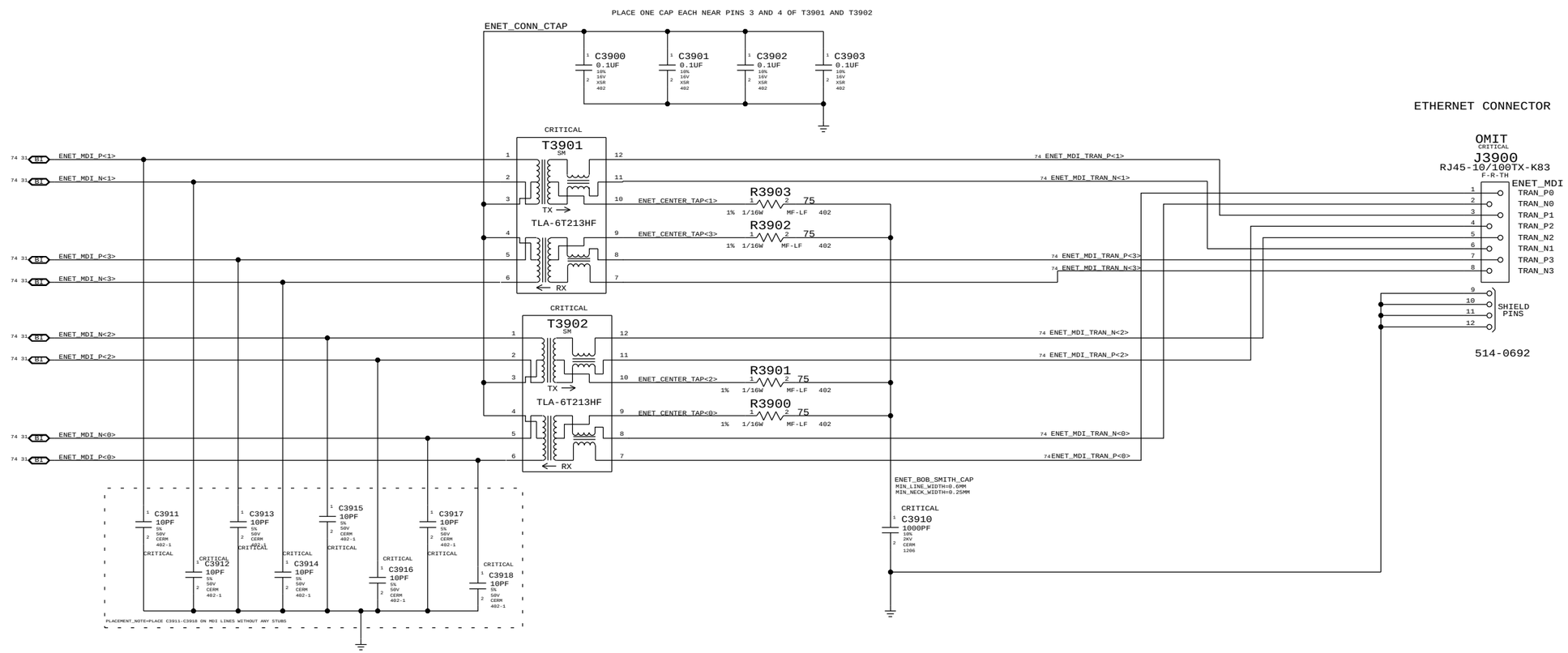
- COPY THIS PAGE FROM K36 CSA.39



SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

PAGE TITLE
ETHERNET CONNECTOR

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

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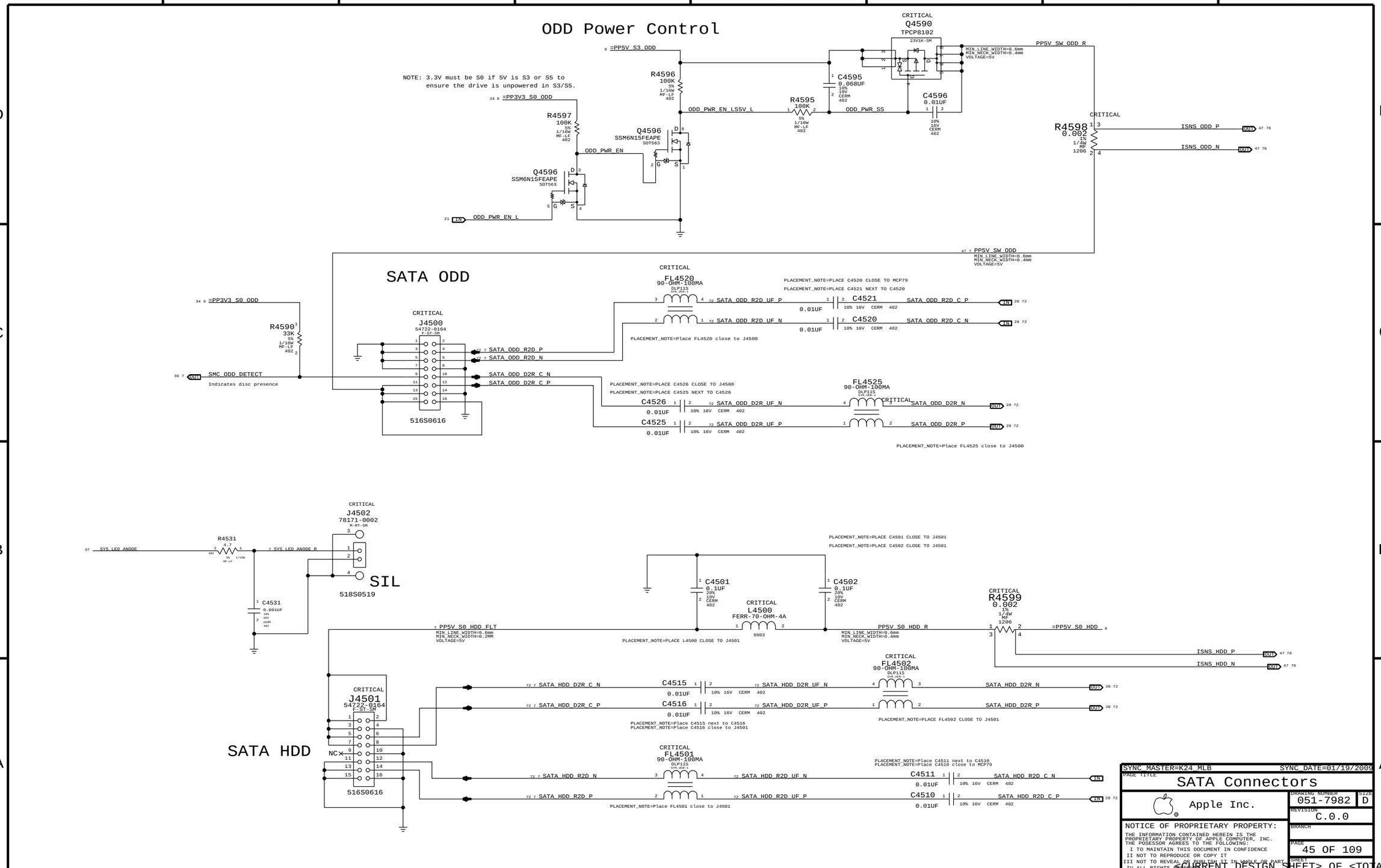

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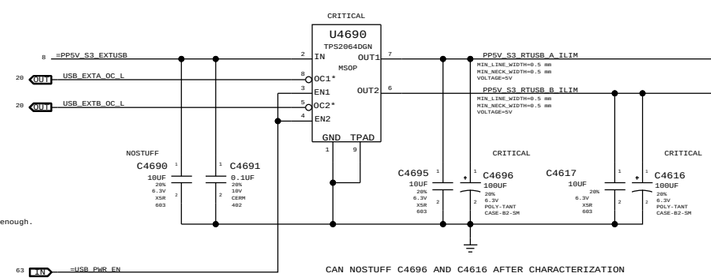
POR IS PLASTIC USB CONNECTOR PARTS BUT METAL PART'S SCHEMATIC AND CAD SYMBOLS
HAVE BEEN USED AS ITS LAND PATTERN CAN ACCOMODATE BOTH TYPES

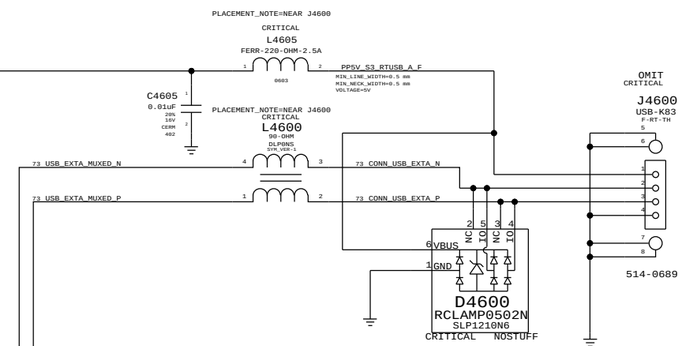
Port Power Switch



We can remove C4690 later if the output cap of the 5V_S5 regulator is close enough.

CAN NOSTUFF C4696 AND C4616 AFTER CHARACTERIZATION

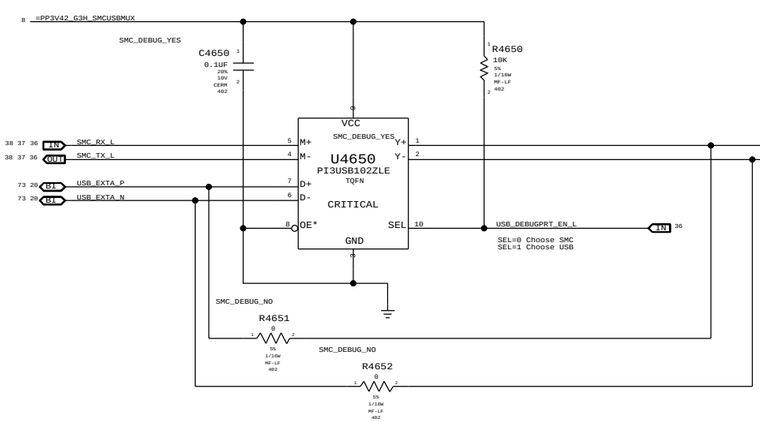
USB PORT A (FRONT PORT)



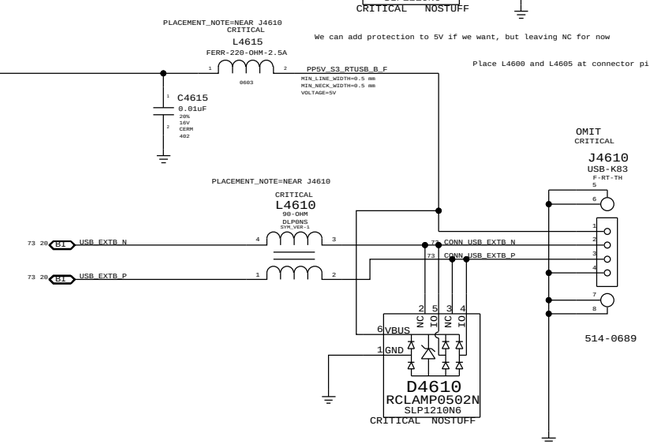
We can add protection to 5V if we want, but leaving NC for now

Place L4600 and L4605 at connector pin

USB/SMC Debug Mux



USB PORT B (BACK PORT)



SYNC_MASTER=K24_MLB SYNC_DATE=02/05/2009

PAGE TITLE
External USB Connectors

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

REVISION C.0.0

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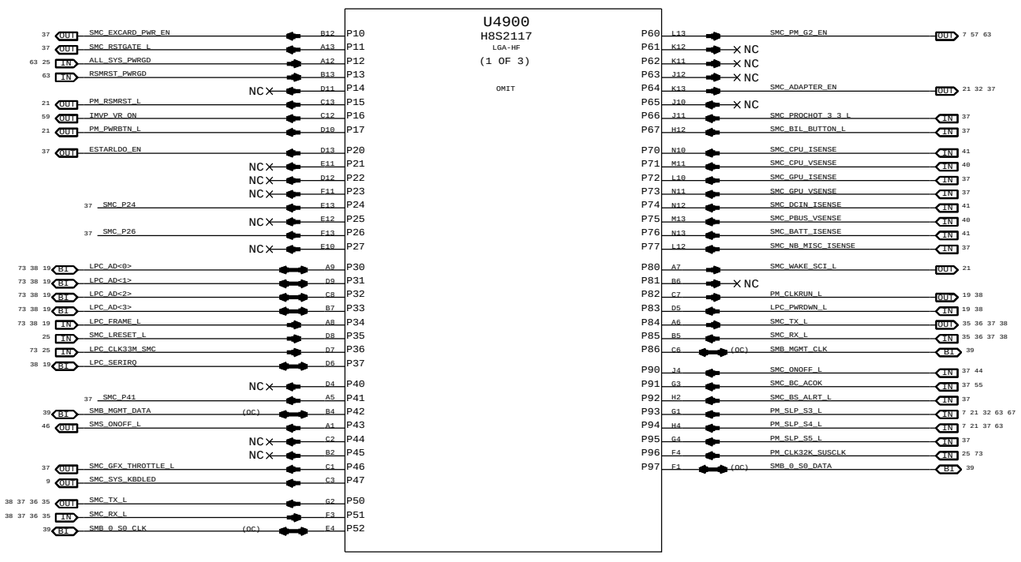
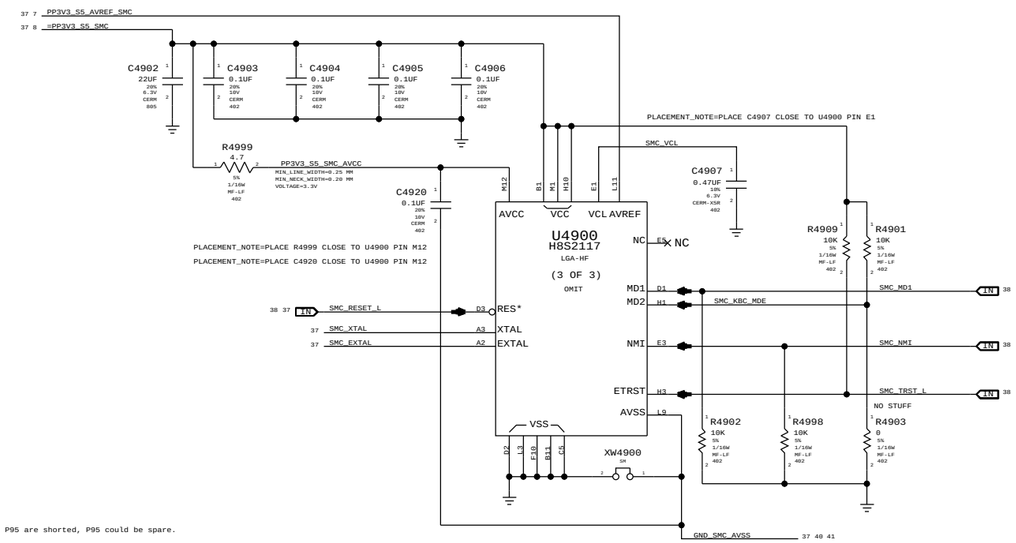
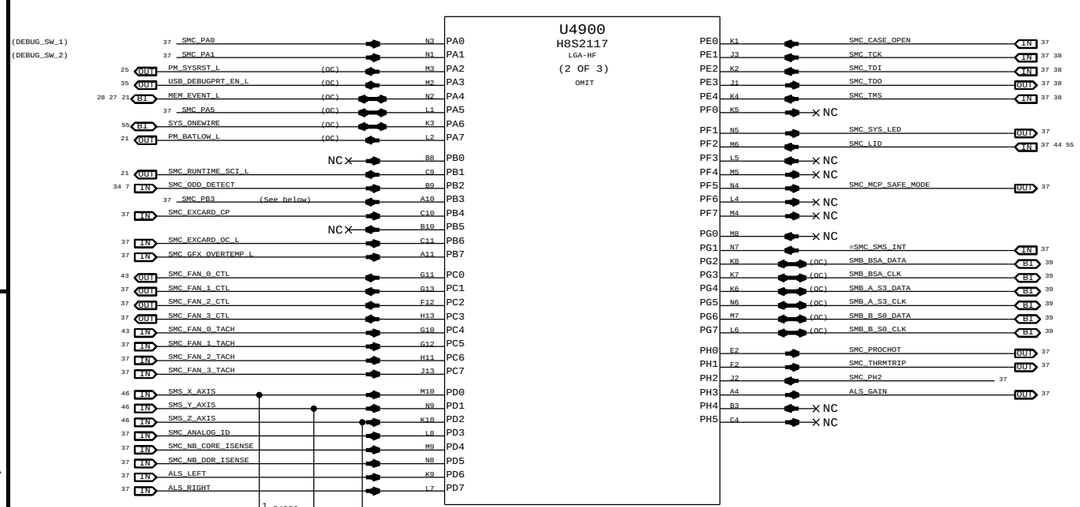
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designed as inputs require pull-ups.





NOTE: P94 and P95 are shorted, P95 could be spare.



PLACEMENT_NOTE=PLACE C4950 CLOSE TO U4900 PIN M10
PLACEMENT_NOTE=PLACE C4951 CLOSE TO U4900 PIN N9
PLACEMENT_NOTE=PLACE C4952 CLOSE TO U4900 PIN K10

SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC_MASTER=K24_MLB SYNC_DATE=04/02/2009

PAGE TITLE
SMC

Apple Inc.

DRAWING NUMBER 051-7982
SIZE D
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PAGE 49 OF 109
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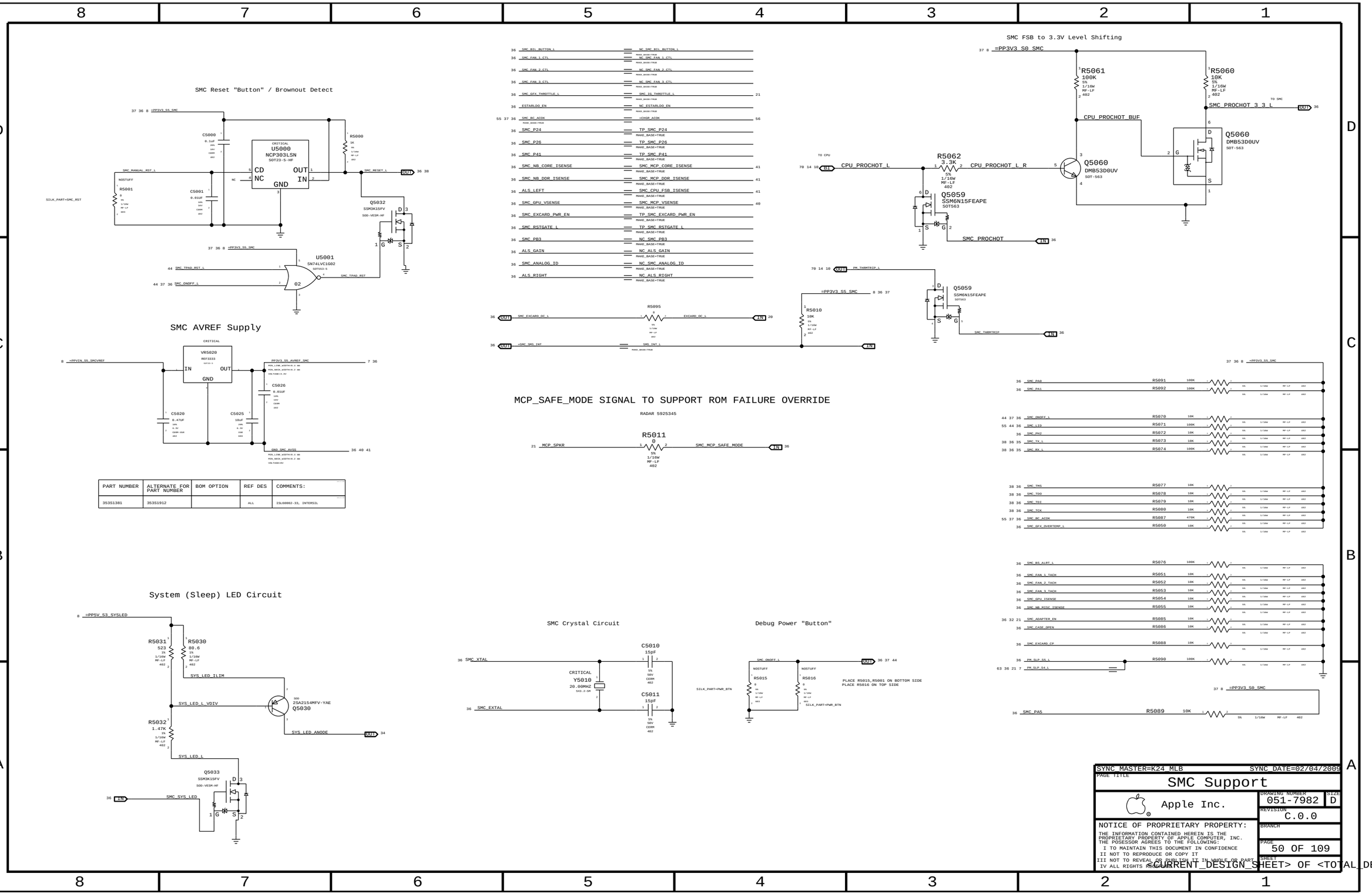

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	ISL60002-33, INTERSIL

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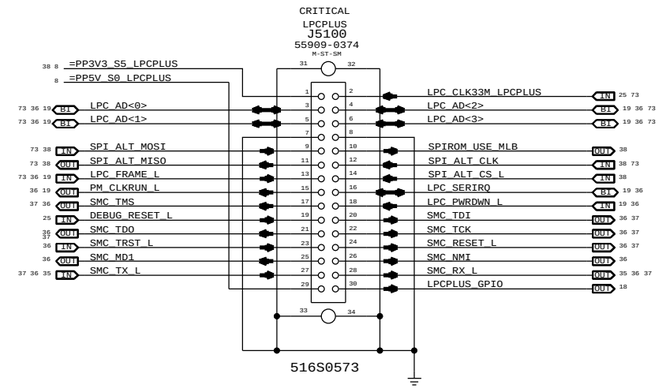
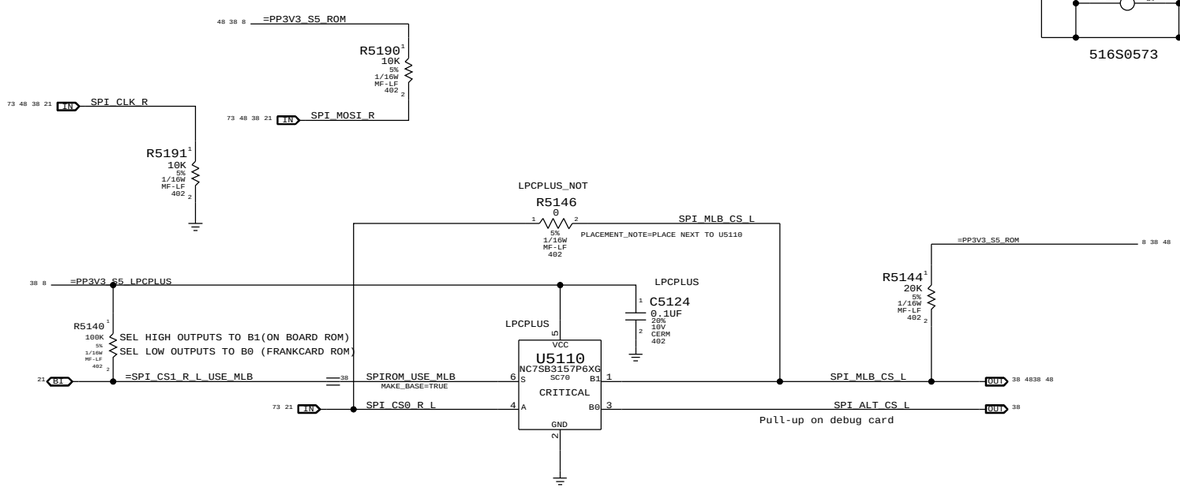
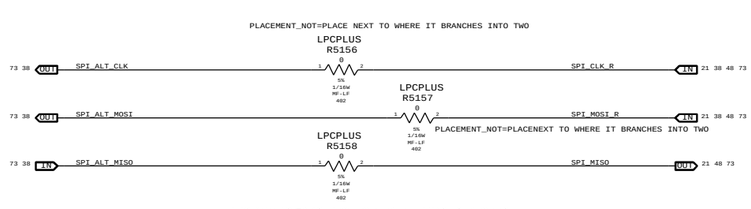
LPC+SPI Connector



Alternate SPI ROM Support





SYNC MASTER=K24 MLB SYNC DATE=02/15/2009

PAGE TITLE
LPC+SPI Debug Connector

Apple Inc.

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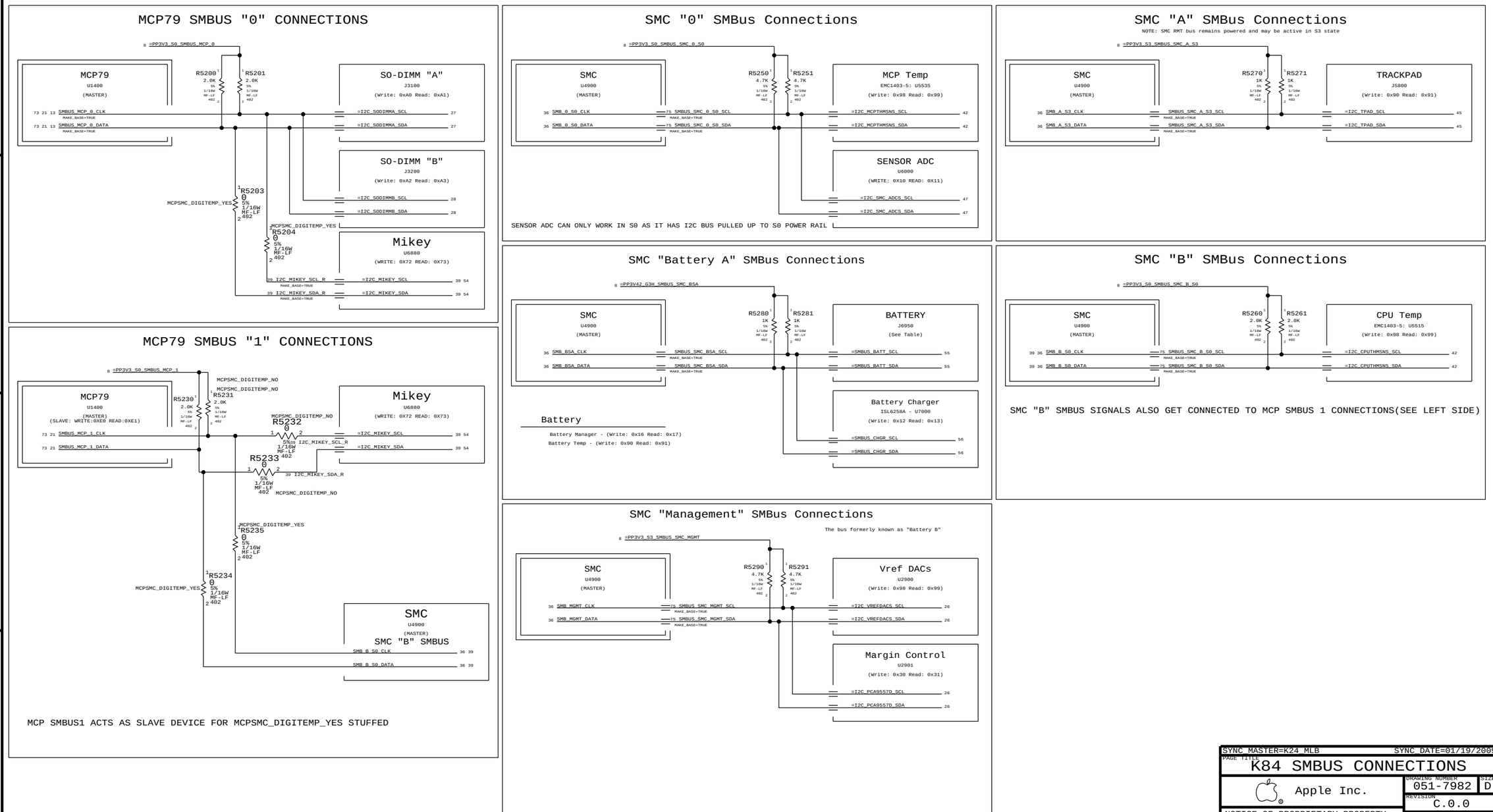

SYNC MASTER=K24 MLB SYNC DATE=01/19/2009

PAGE TITLE
K84 SMBUS CONNECTIONS

Apple Inc.

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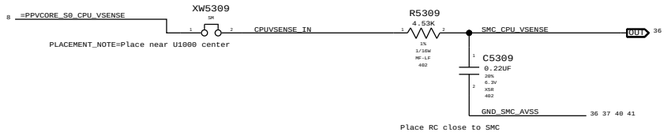
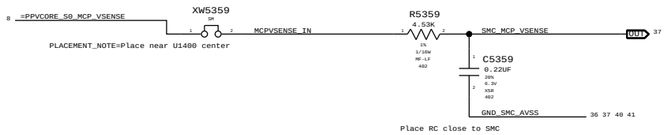
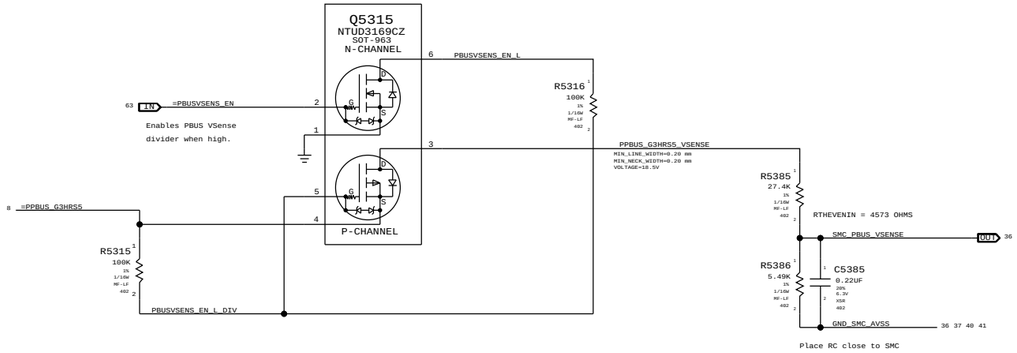
CPU Voltage Sense / Filter



MCP Voltage Sense / Filter



PBUS VOLTAGE SENSE ENABLE & FILTER



SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

PAGE TITLE
VOLTAGE SENSING

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

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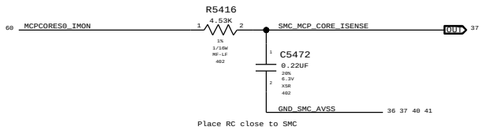
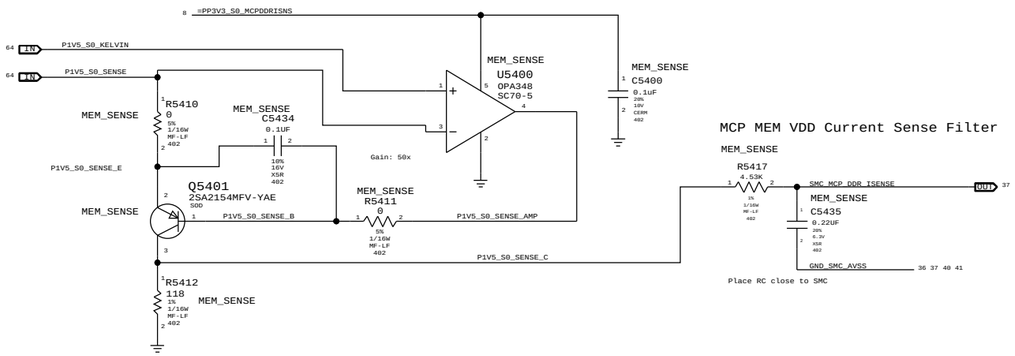
MCP VCore Current Sense Filter

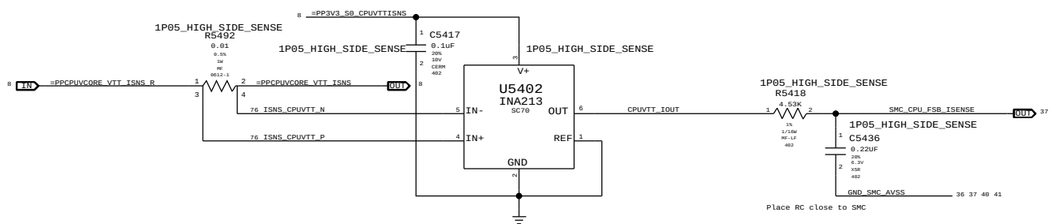


MCP MEM VDD Current Sense

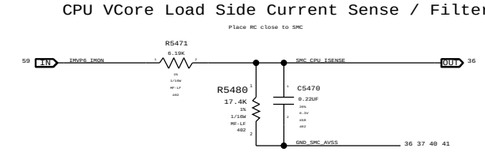


MCP MEM VDD Current Sense Filter

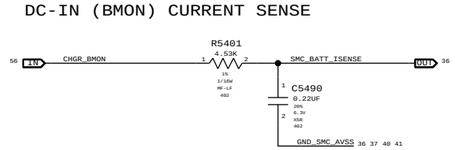
CPU 1.05V AND CPU VCORE HIGH SIDE CURRENT SENSE



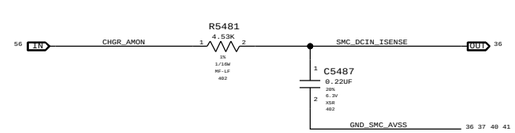
CPU VCore Load Side Current Sense / Filter



DC-IN (BMON) CURRENT SENSE



DC-IN (AMON) CURRENT SENSE



SYNC MASTER=K24 MLB SYNC DATE=01/27/2009

PAGE TITLE
Current Sensing

Apple Inc.

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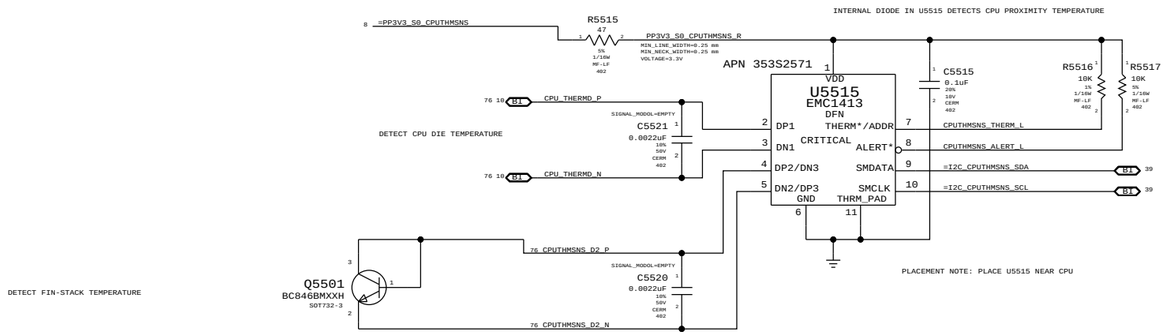
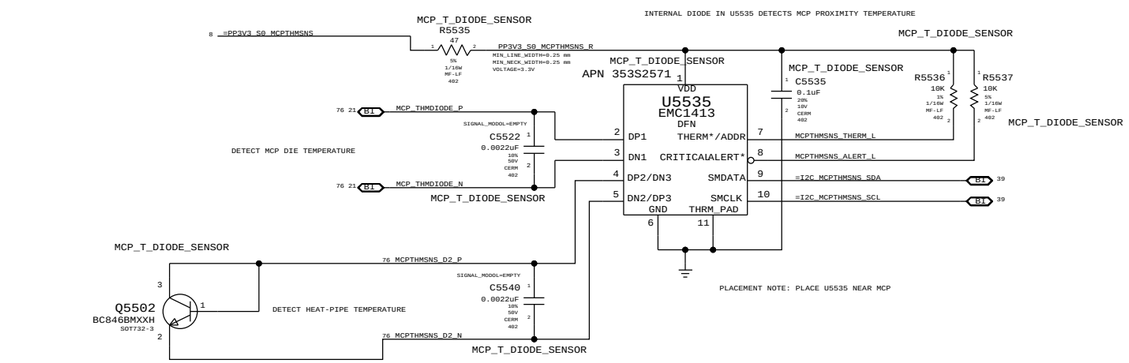
CPU T-Diode Thermal Sensor



MCP T-Diode Thermal Sensor



PLACEMENT_NOTE=PLACE CLOSE TO J4501 IN A CONVENIENT LOCATION

SYNC_MASTER=K24_MLB SYNC_DATE=02/04/2009

PAGE TITLE
Thermal Sensors

Apple Inc.

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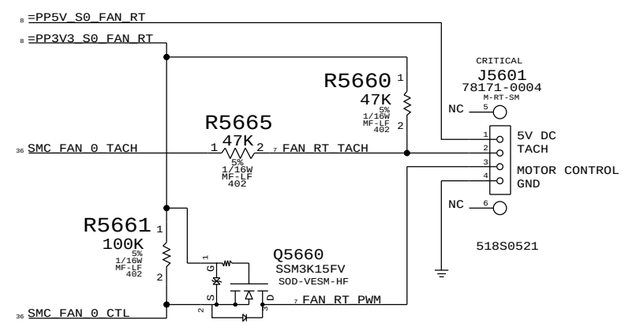

SYNC_MASTER=K24_MLB SYNC_DATE=04/06/2009

PAGE TITLE

Fan

Apple Inc.

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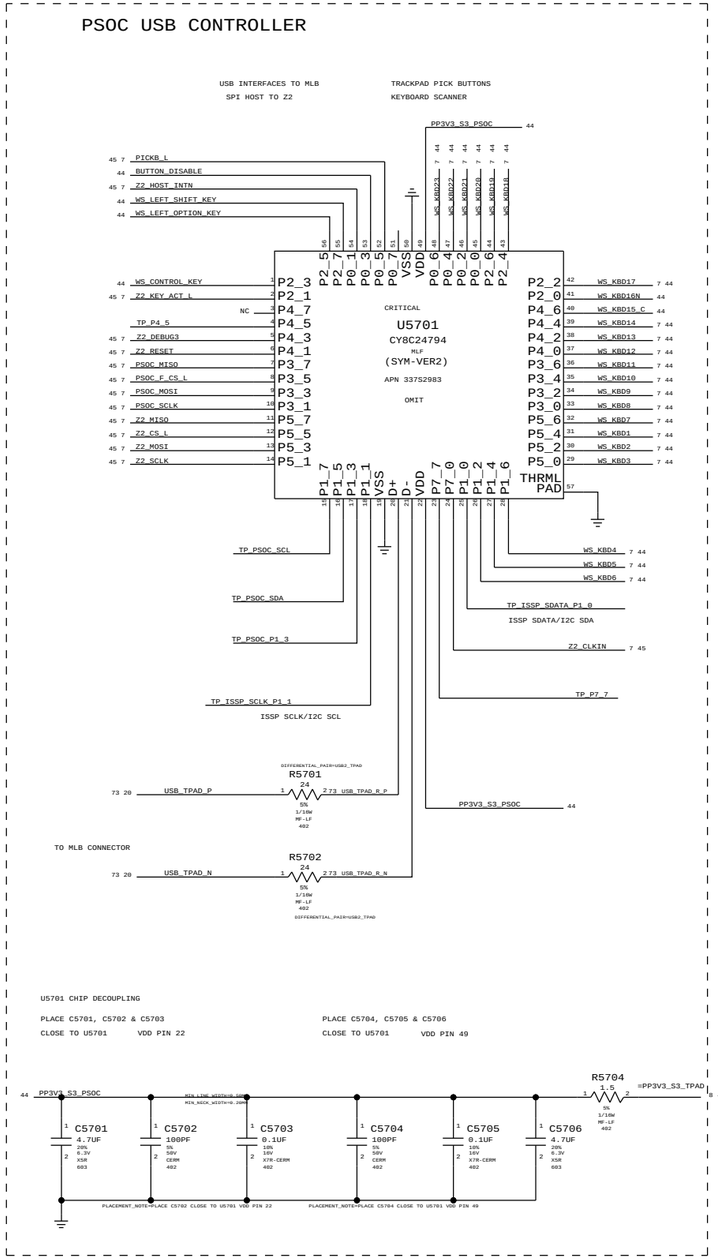
PSOC USB CONTROLLER



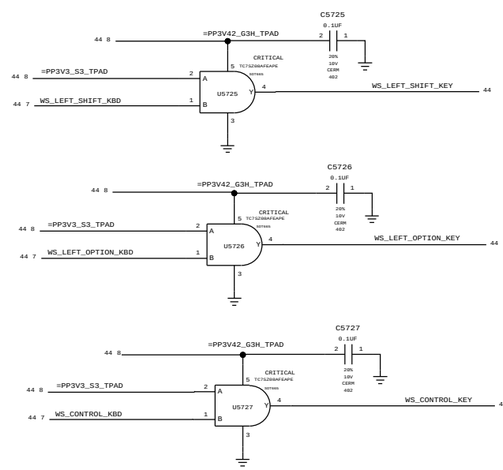
U5701 CHIP DECOUPLING

PLACE C5701, C5702 & C5703
CLOSE TO U5701 VDD PIN 22

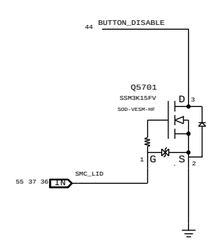
PLACE C5704, C5705 & C5706
CLOSE TO U5701 VDD PIN 49

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA MAX	10 OHM	0.6 V	36E-3 W
	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

ISOLATION CIRCUIT



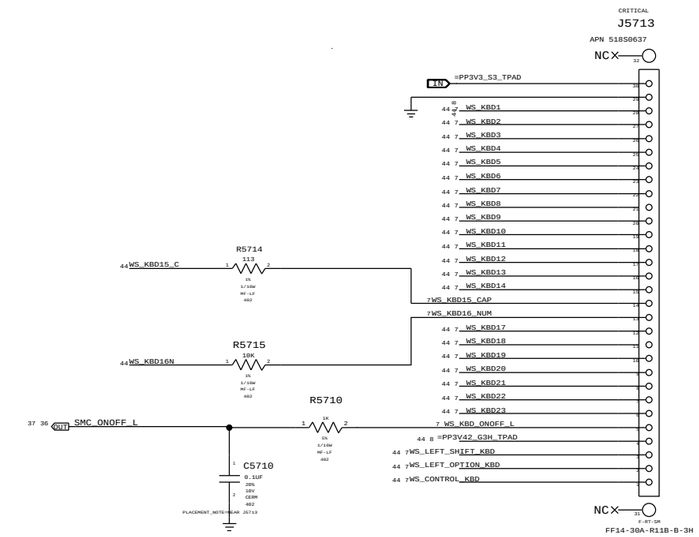
TPAD BUTTONS DISABLE



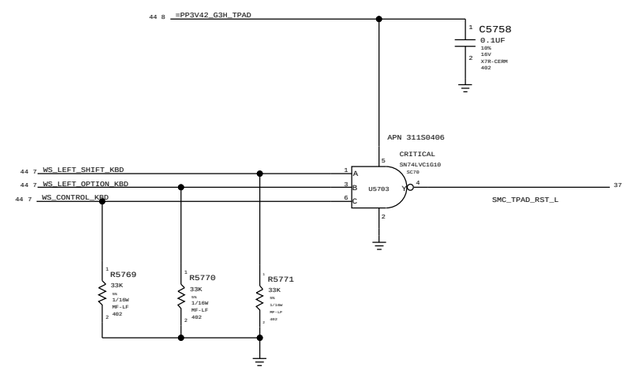
PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

KEYBOARD CONNECTOR



SMC_MANUAL_RESET LOGIC



Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0406	311S0447		ALL	NXP PART AS ALTERNATE

SYNC MASTER=K24 MLB SYNC DATE=03/04/2009

PAGE TITLE
WELLSPRING 1

Apple Inc.

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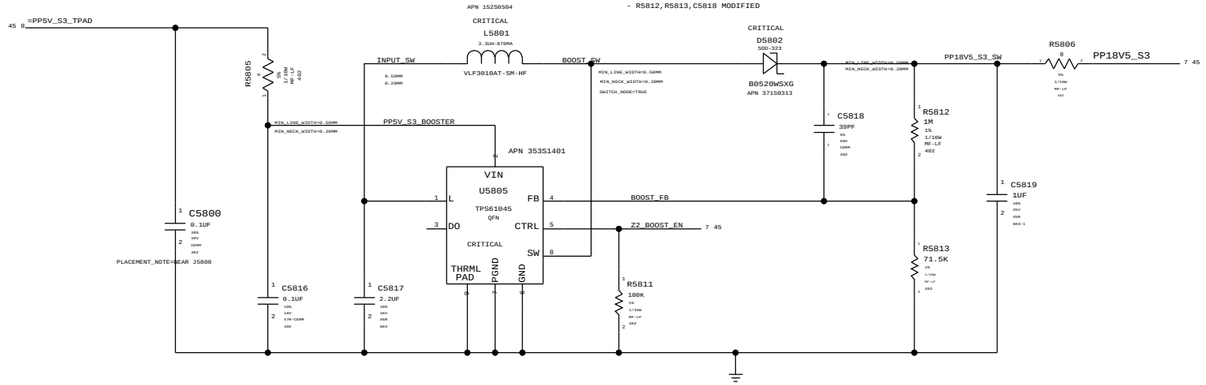
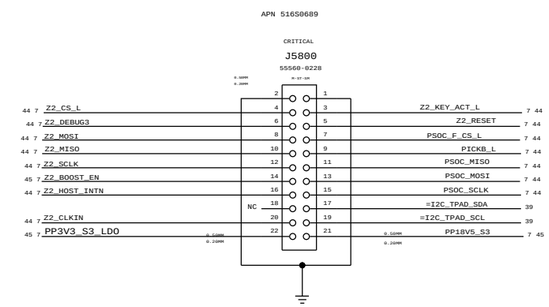
BOOSTER +18.5VDC FOR SENSORS

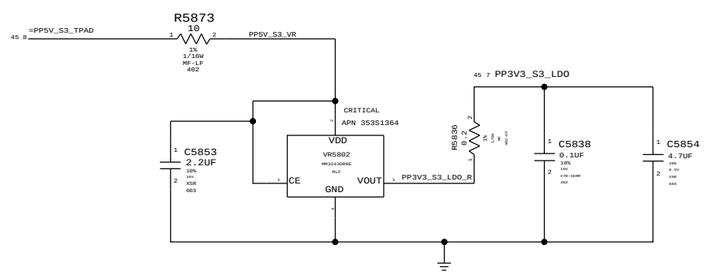
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD FLEX CONNECTOR



3V3 LDO FOR IPD



SYNC MASTER=K24 MLB SYNC DATE=02/25/2009

PAGE TITLE
WELLSPRING 2

Apple Inc.

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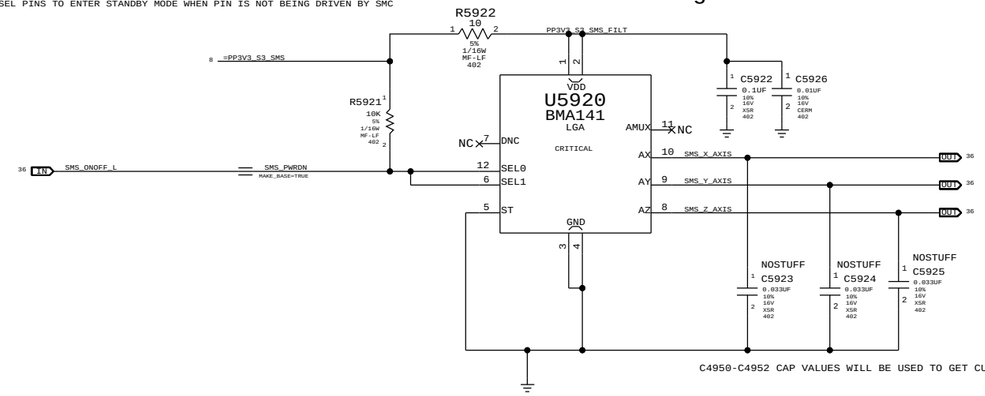
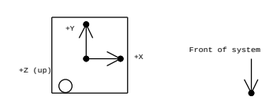
Analog SMS

R5921 PULLS UP SEL PINS TO ENTER STANDBY MODE WHEN PIN IS NOT BEING DRIVEN BY SMC



Desired orientation when placed on board top-side:



Circle indicates pin 1 location when placed in correct orientation

C4950-C4952 CAP VALUES WILL BE USED TO GET CUT-OFF FREQUENCY OF ~146HZ

PAGE TITLE	SMS
Apple Inc.	DRAWING NUMBER 051-7982 SIZE D
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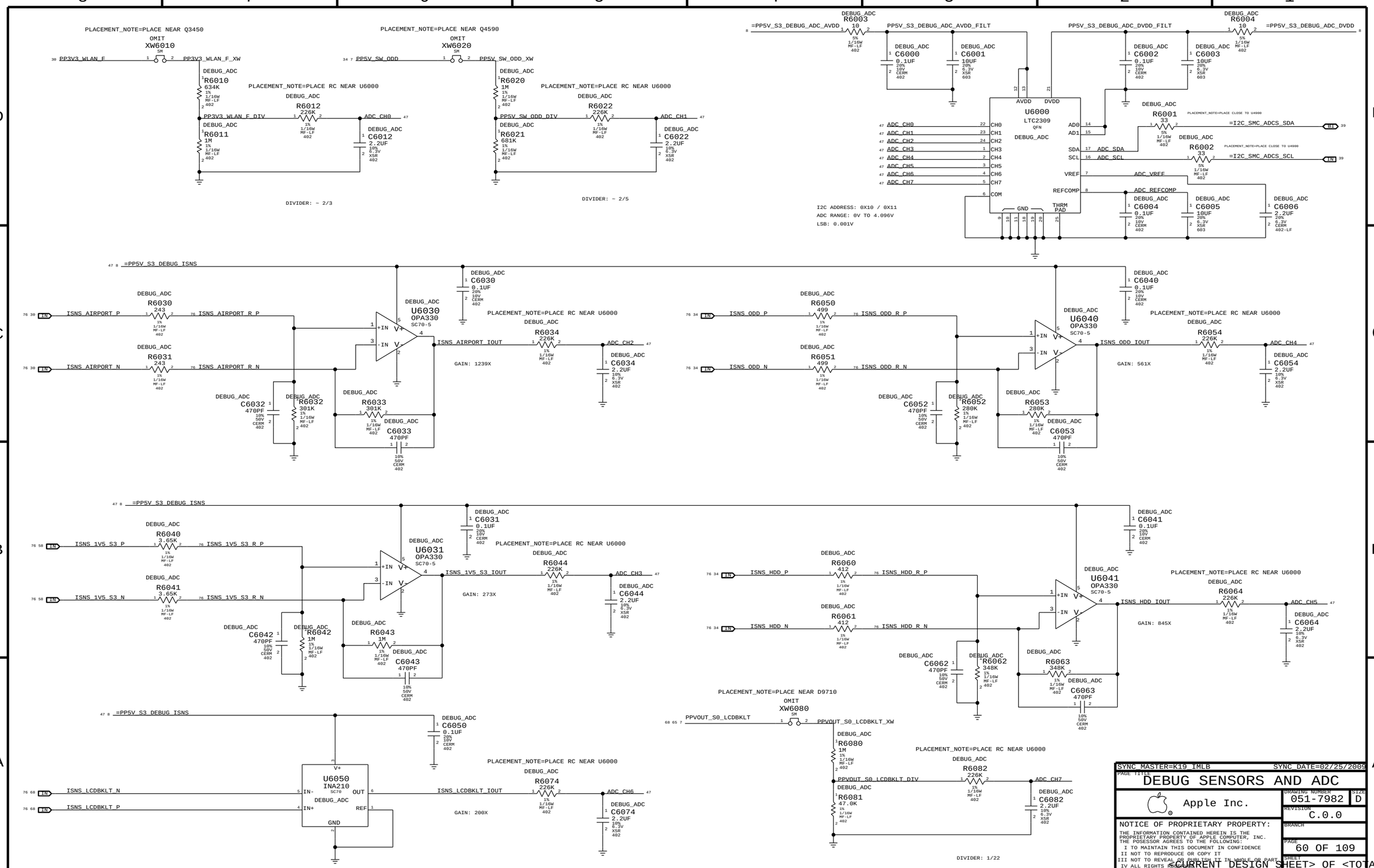

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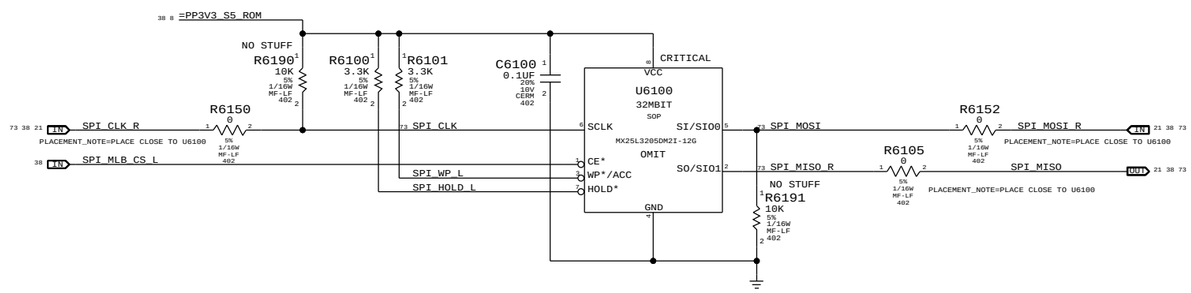

MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
Any of the 4 frequencies can be selected
with R6190, R6191, R5190 and R5191

SYNC MASTER=K24 MLB SYNC DATE=02/15/2009

PAGE TITLE
SPI ROM

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D
REVISION C.0.0
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PAGE 61 OF 109
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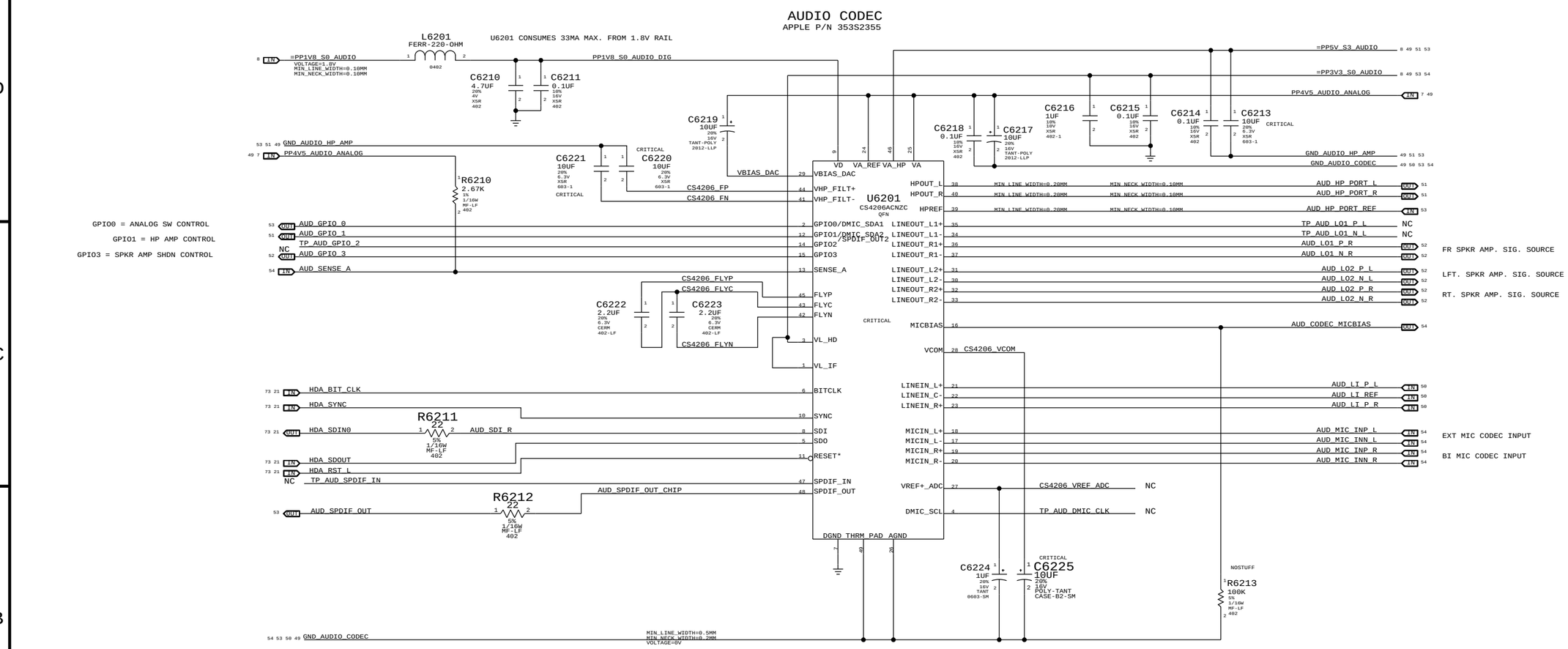
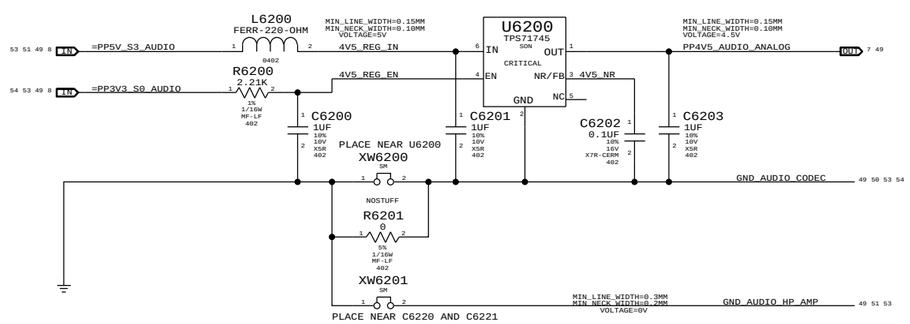


4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456



NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC_MASTER=AUDIO SYNC_DATE=06/09/2009

PAGE TITLE: AUDIO: CODEC/REGULATOR	
Apple Inc.	DRAWING NUMBER: 051-7982 SIZE: D
	REVISION: C.0.0
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	PAGE: 62 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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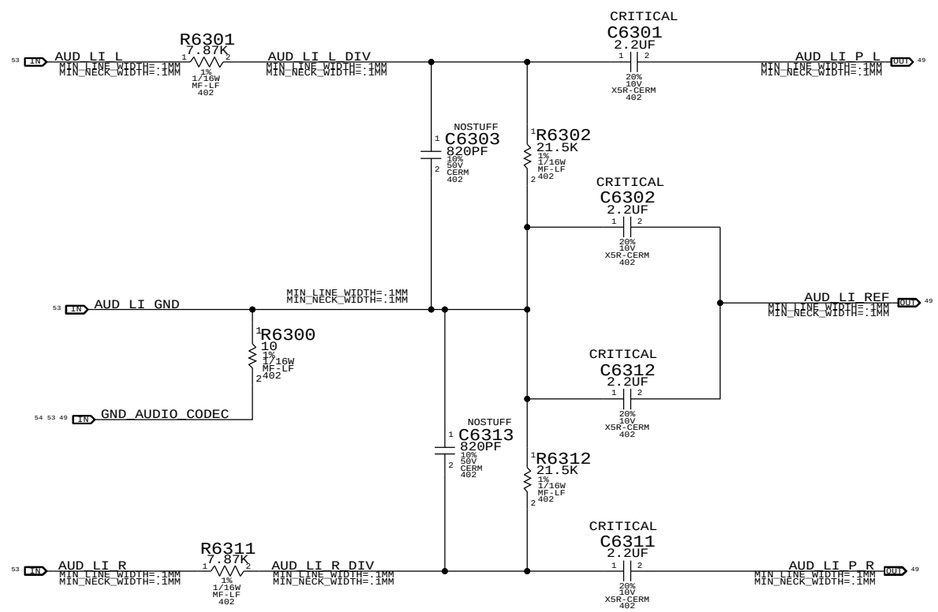
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
FC_HP = 3.6 HZ
FC_LP = 43KHZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS



PAGE TITLE
AUDIO: LINE INPUT FILTER

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D
REVISION C.0.0
BRANCH
PAGE 63 OF 109
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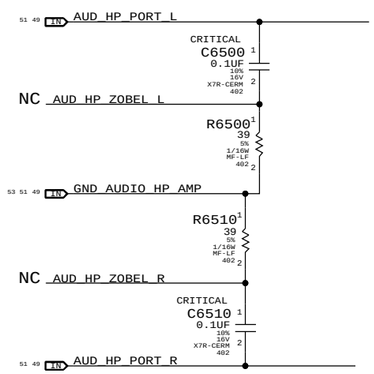

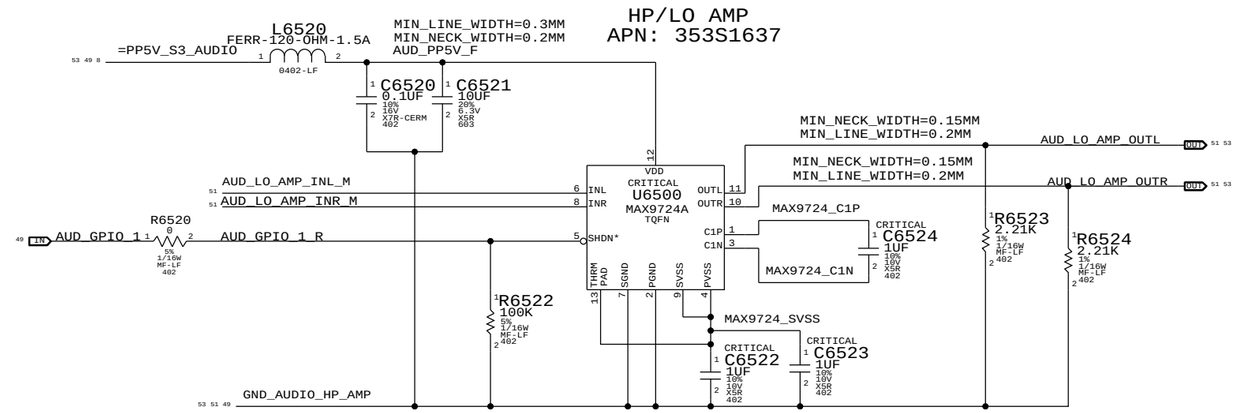

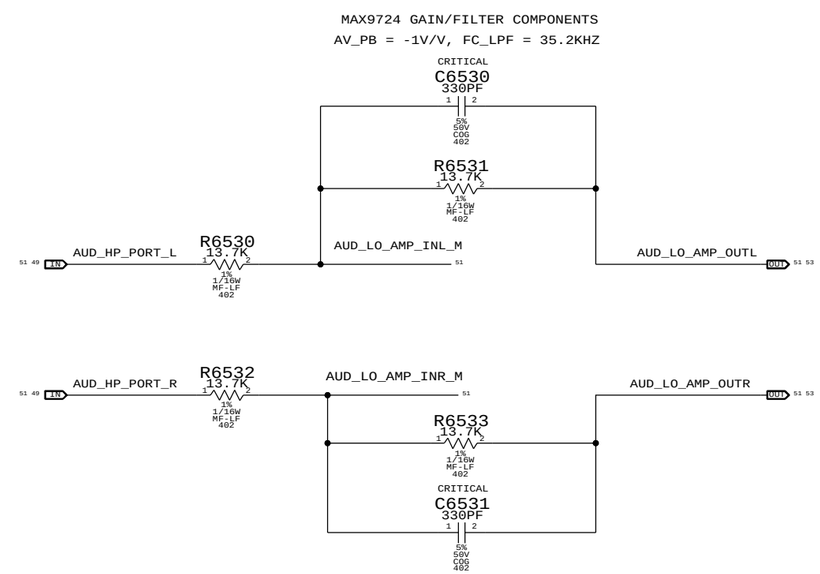

SYNC MASTER=AUDIO SYNC DATE=06/09/2009

PAGE TITLE
AUDIO: HEADPHONE FILTER

Apple Inc.

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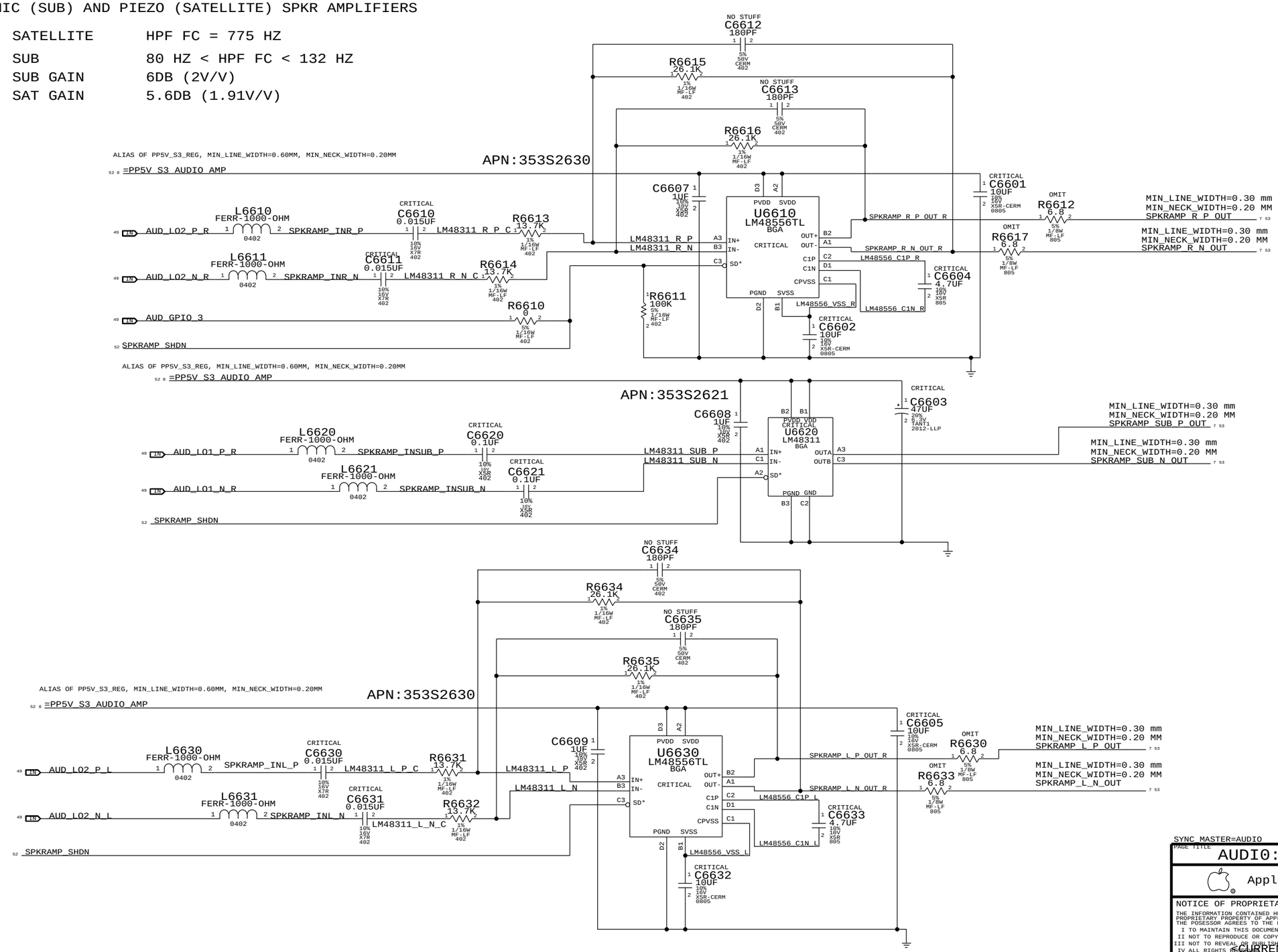
DYNAMIC (SUB) AND PIEZO (SATELLITE) SPKR AMPLIFIERS

SATELLITE	HPF FC = 775 HZ
SUB	80 HZ < HPF FC < 132 HZ
SUB GAIN	6DB (2V/V)
SAT GAIN	5.6DB (1.91V/V)



SYNC_MASTER=AUDIO SYNC_DATE=06/09/2009

PAGE TITLE: AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER: 051-7982 SIZE: D

REVISION: C.0.0

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PAGE: 66 OF 109

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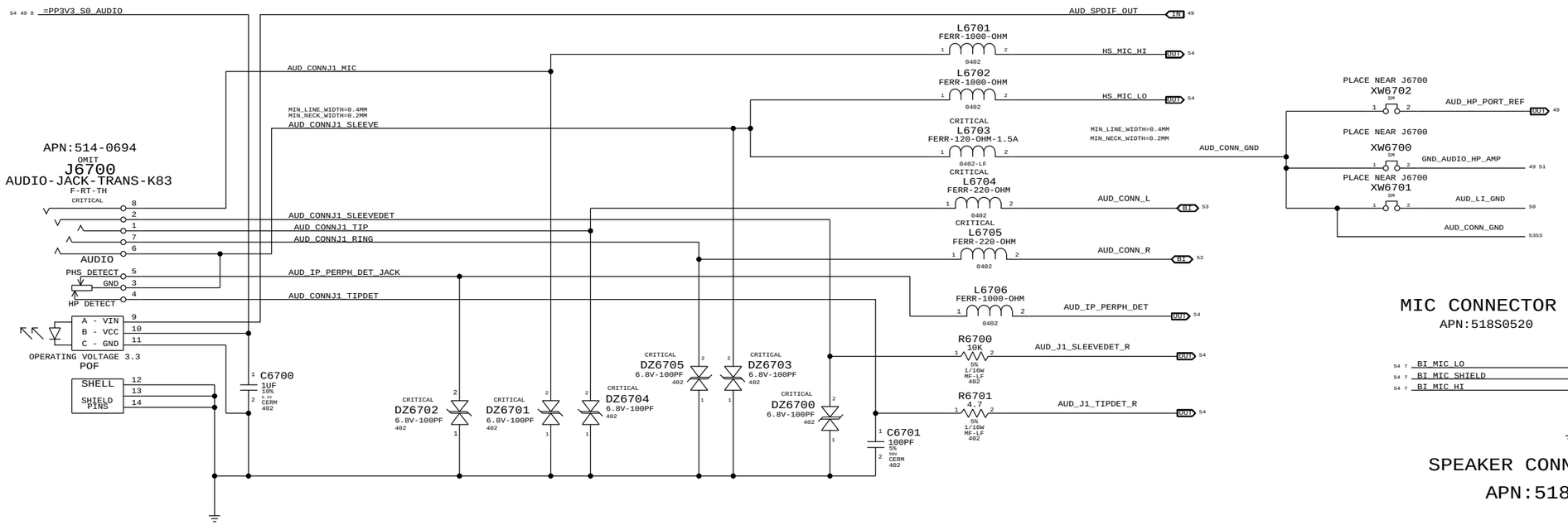
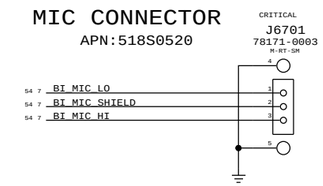
AUDIO JACK: LI/LO/HP CONNECTOR, SPDIF TX



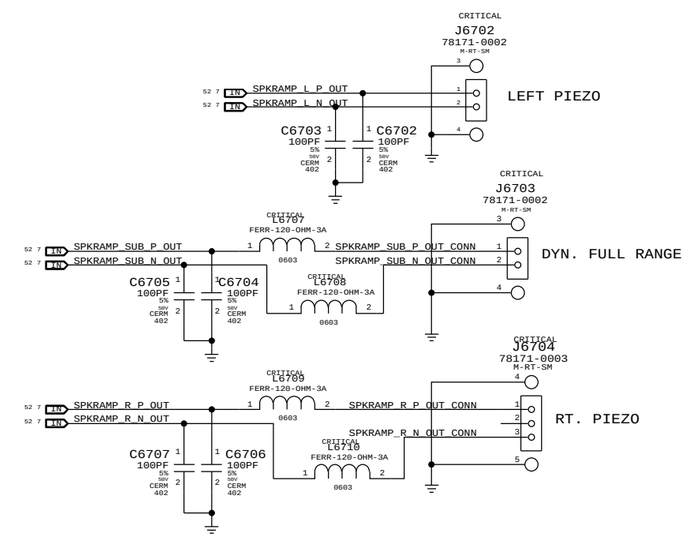
MIC CONNECTOR

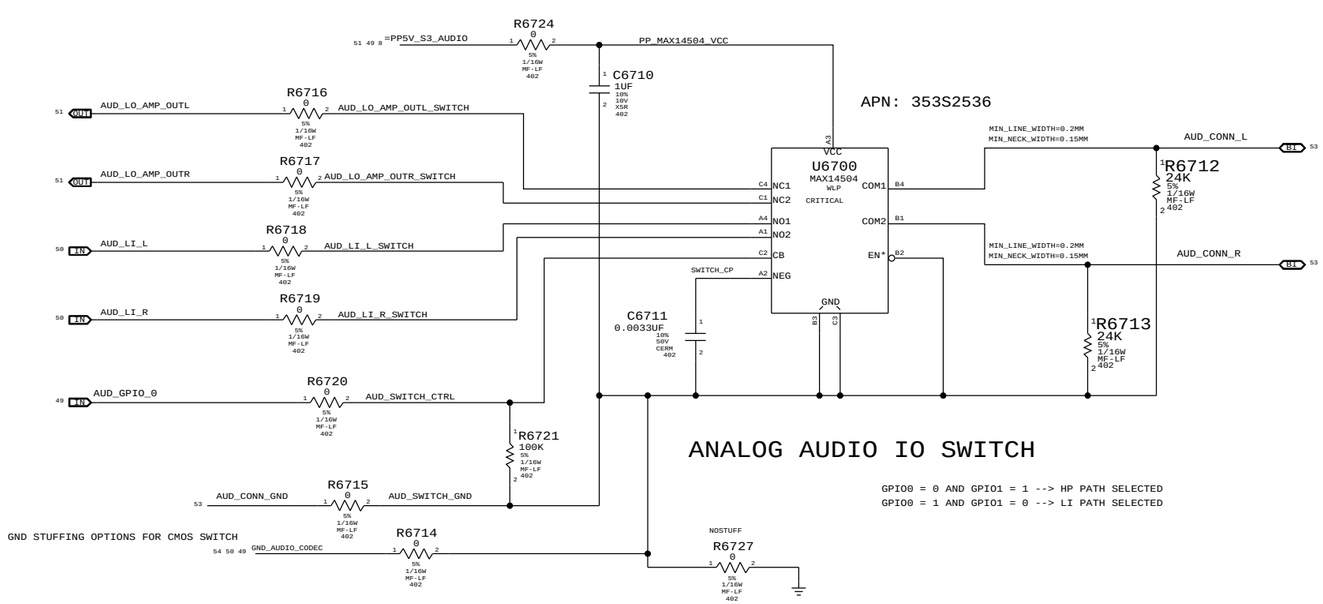
APN:518S0520



SPEAKER CONNECTORS

APN:518S0519





ANALOG AUDIO IO SWITCH

GPIO0 = 0 AND GPIO1 = 1 --> HP PATH SELECTED
GPIO0 = 1 AND GPIO1 = 0 --> LI PATH SELECTED

SYNC_MASTER=AUDIO SYNC_DATE=06/09/2009

PAGE TITLE: AUDIO: JACK

Apple Inc.

DRAWING NUMBER: 051-7982 SIZE: D

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CODEC OUTPUT SIGNAL PATHS

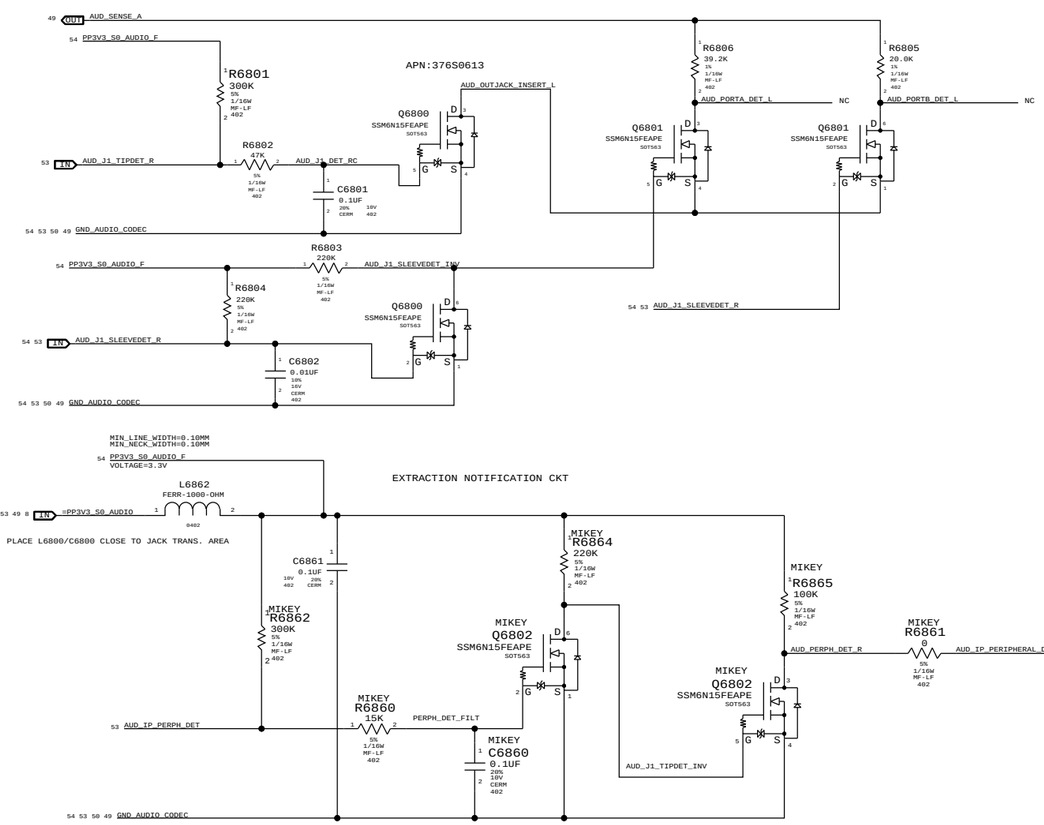
FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	GPIO_0 AND GPIO_1	0X09 (A)
LINE IN	0X05 (5)	0X05 (5)	0X0C (12)	GPIO_0 AND GPIO_1	0X09 (A) AND UI ELEMENT
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0D (B)

CODEC INPUT SIGNAL PATHS

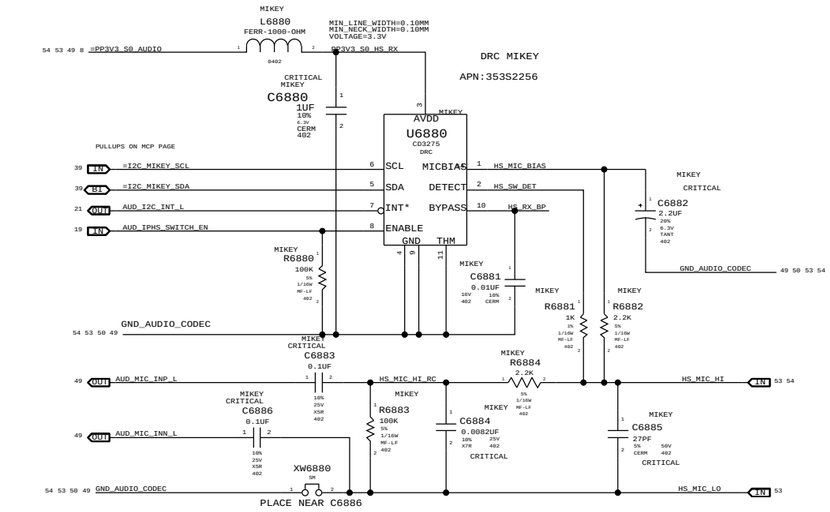
FUNCTION	CONVERTER	PIN COMPLEX	VREF/ENABLE	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MCP79 GPIO_38	MCP79 GPIO_17 (PERIPH DETECT) MCP79 GPIO_4 (LOAD DETECT)

PORT A DETECT (HEADPHONES)

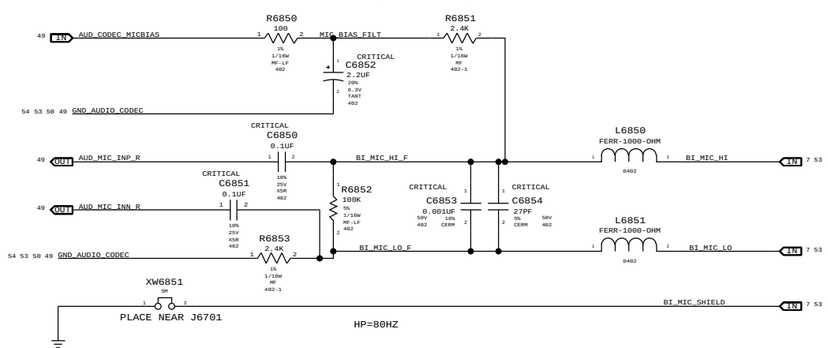
PORT B DETECT(SPDIF DELEGATE)



PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=8.82KHZ

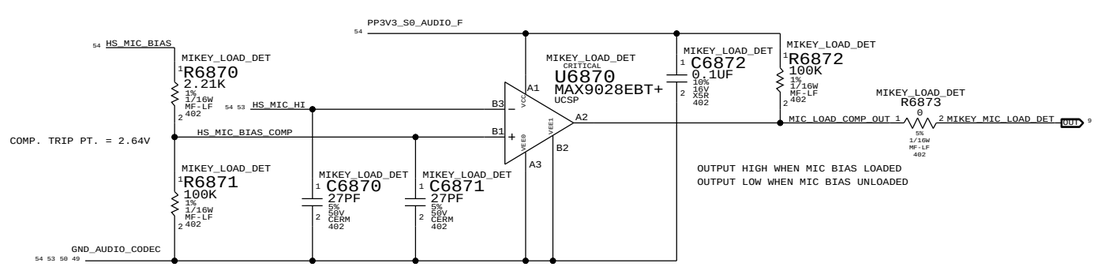


PORT B RIGHT(BUILT-IN MIC)



EXTRACTION NOTIFICATION CKT

MIKEY MIC LOAD DET CKT



SYNC MASTER=AUDIO SYNC DATE=06/09/2009

PAGE TITLE
AUDIO: JACK TRANSLATORS

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

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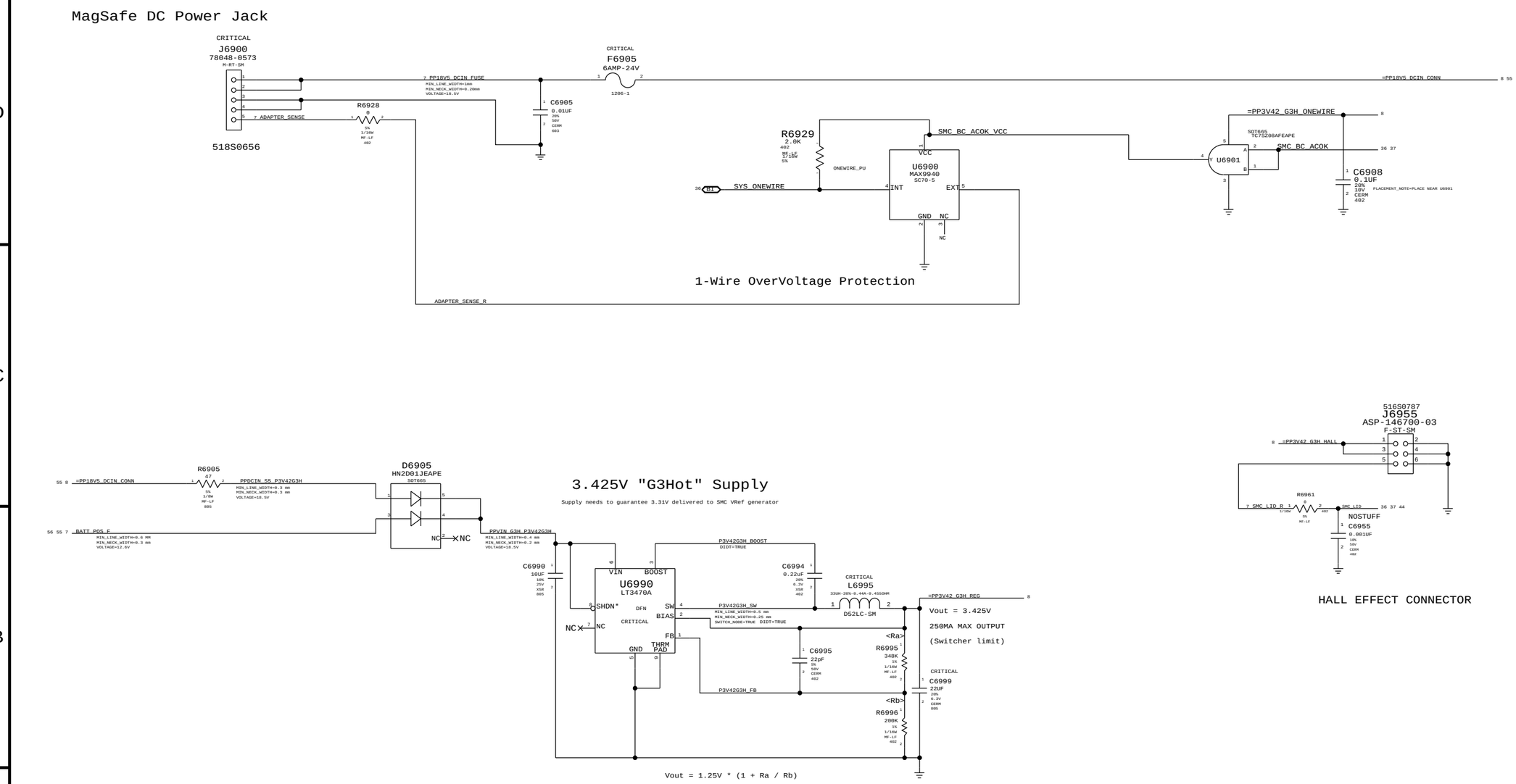

SYNC_MASTER=K24_MLB SYNC_DATE=02/05/2009

PAGE TITLE
DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

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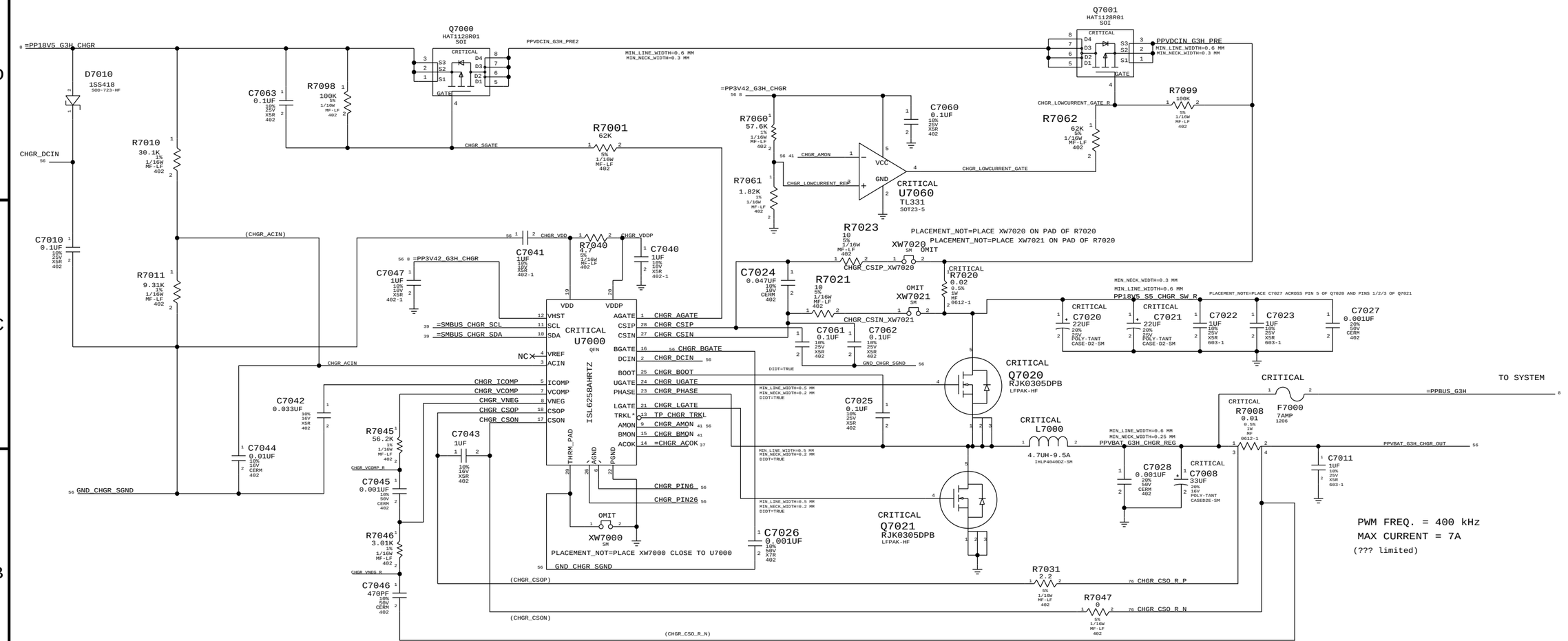
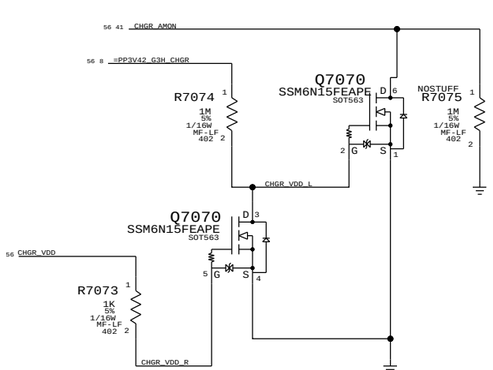
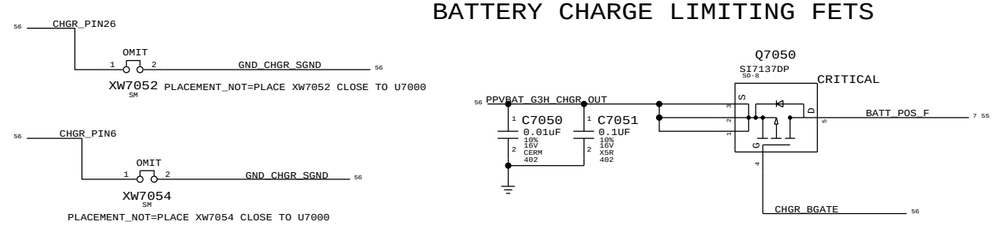
PBUS SUPPLY / BATTERY CHARGER



AMON PULLDOWN LOGIC



BATTERY CHARGE LIMITING FETS



SYNC MASTER=K24 MLB SYNC DATE=02/05/2009

PAGE TITLE
PBUS Supply/Battery Charger

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

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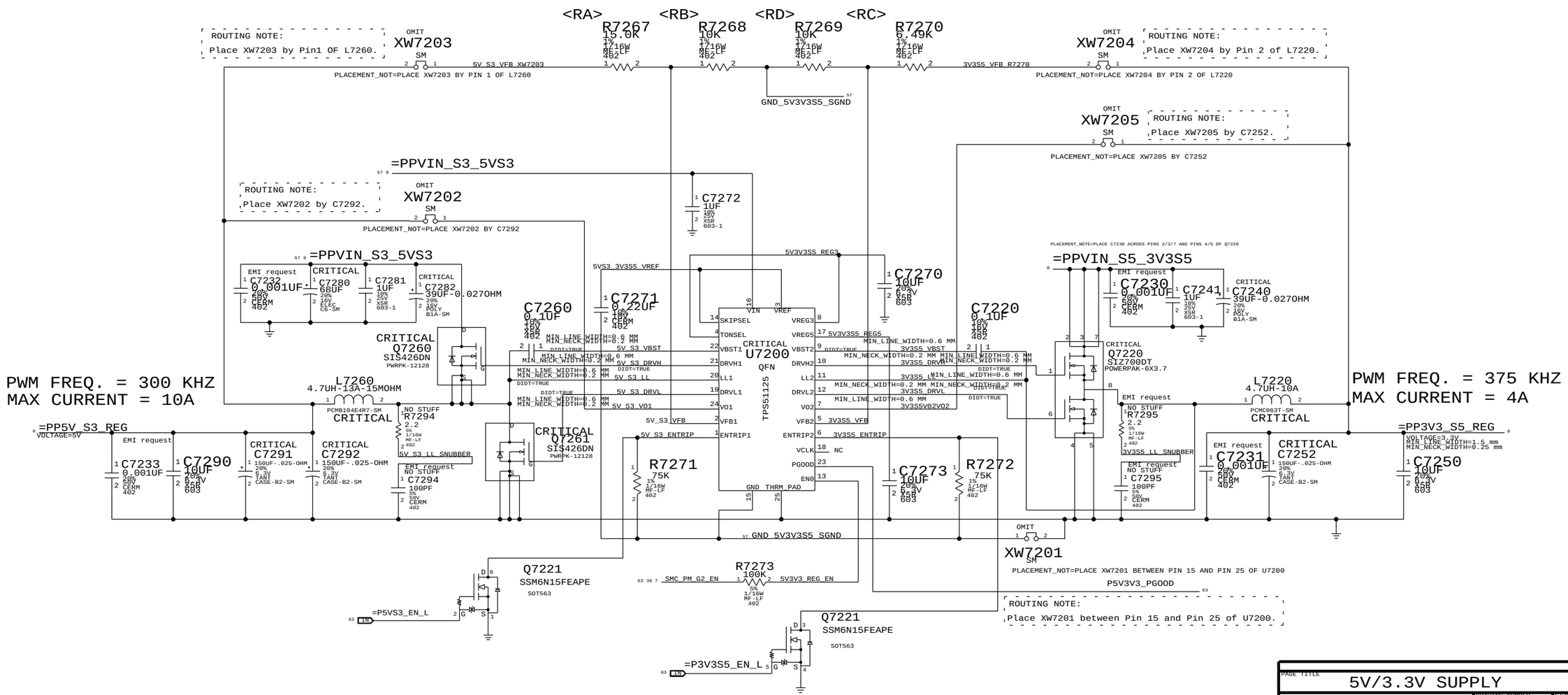
- COPY THIS PAGE FROM K36 CSA.76

5V S3/3.3V S5 POWER SUPPLY

VOUT = (2 * RA / RB) + 2

VOUT = (2 * RC / RD) + 2



PAGE TITLE	5V/3.3V SUPPLY
Apple Inc.	DRAWING NUMBER 051-7982 SIZE D
	REVISION C.0.0
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	PAGE 72 OF 109
	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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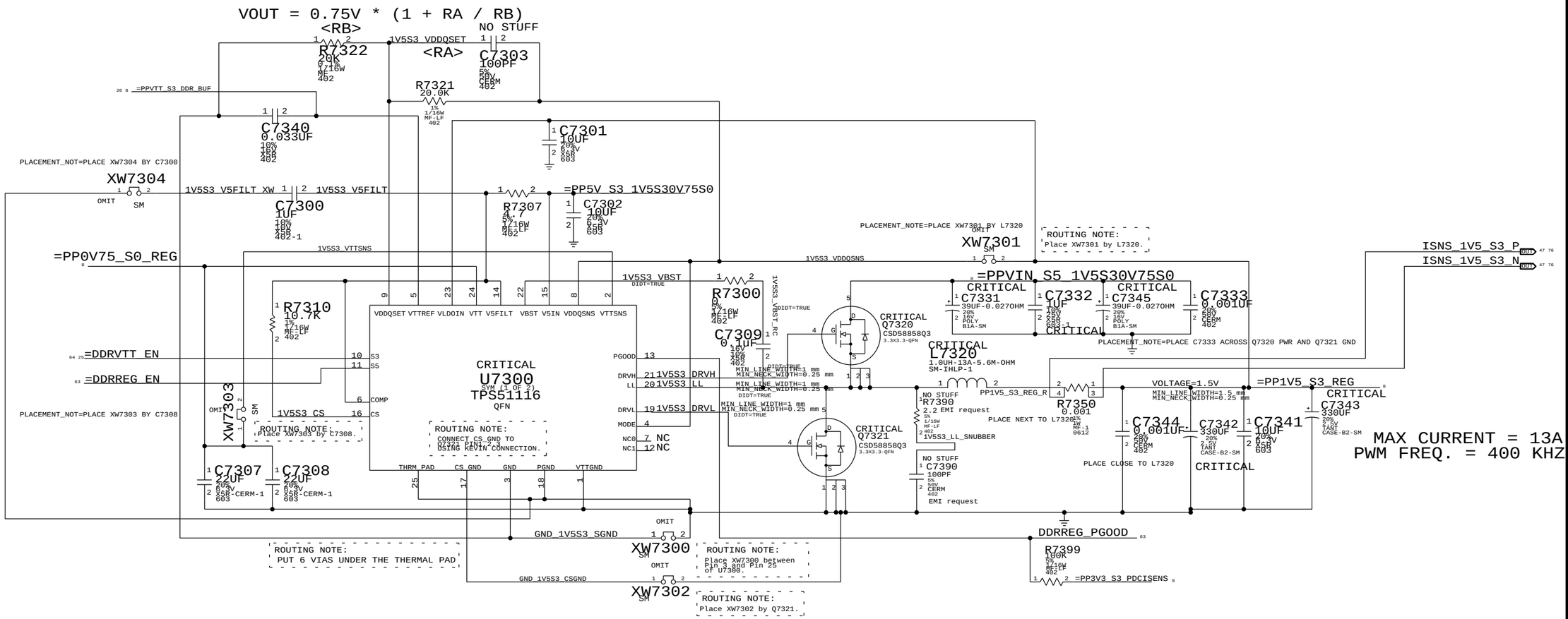
1.5V/0.75V(DDR3) POWER SUPPLY



STATE	PM_SLP_S4_L	PM_SLP_S3_L	PP1V5_S3	PP0V75_S0
S0	HIGH	HIGH	1.5V	0.75V
S3	HIGH	LOW	1.5V	0.0V
S5/G3HOT	LOW	LOW	0.0V	0.0V

PAGE TITLE: 1.5V/0.75V DDR3 SUPPLY

Apple Inc.

DRAWING NUMBER: 051-7982 SIZE: D

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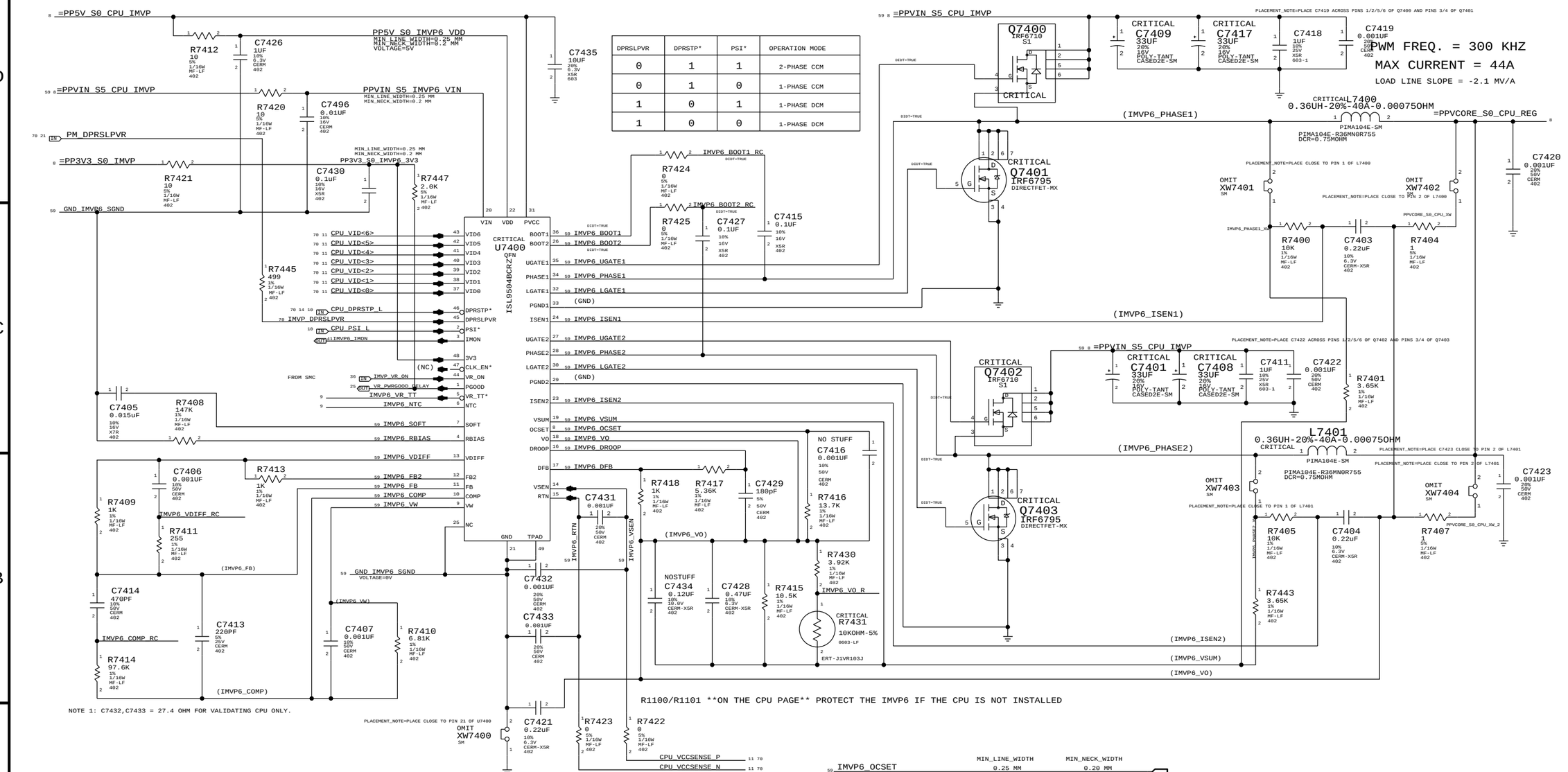

DPRSLPVR	DPRSTP*	PSI*	OPERATION MODE
0	1	1	2-PHASE CCM
0	1	0	1-PHASE CCM
1	0	1	1-PHASE DCM
1	0	0	1-PHASE DCM

IMVP6 CPU VCORE REGULATOR

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM

IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

SYNC MASTER=K24_MLB SYNC DATE=03/03/2009

PAGE TITLE
IMVP6 CPU VCore Regulator

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

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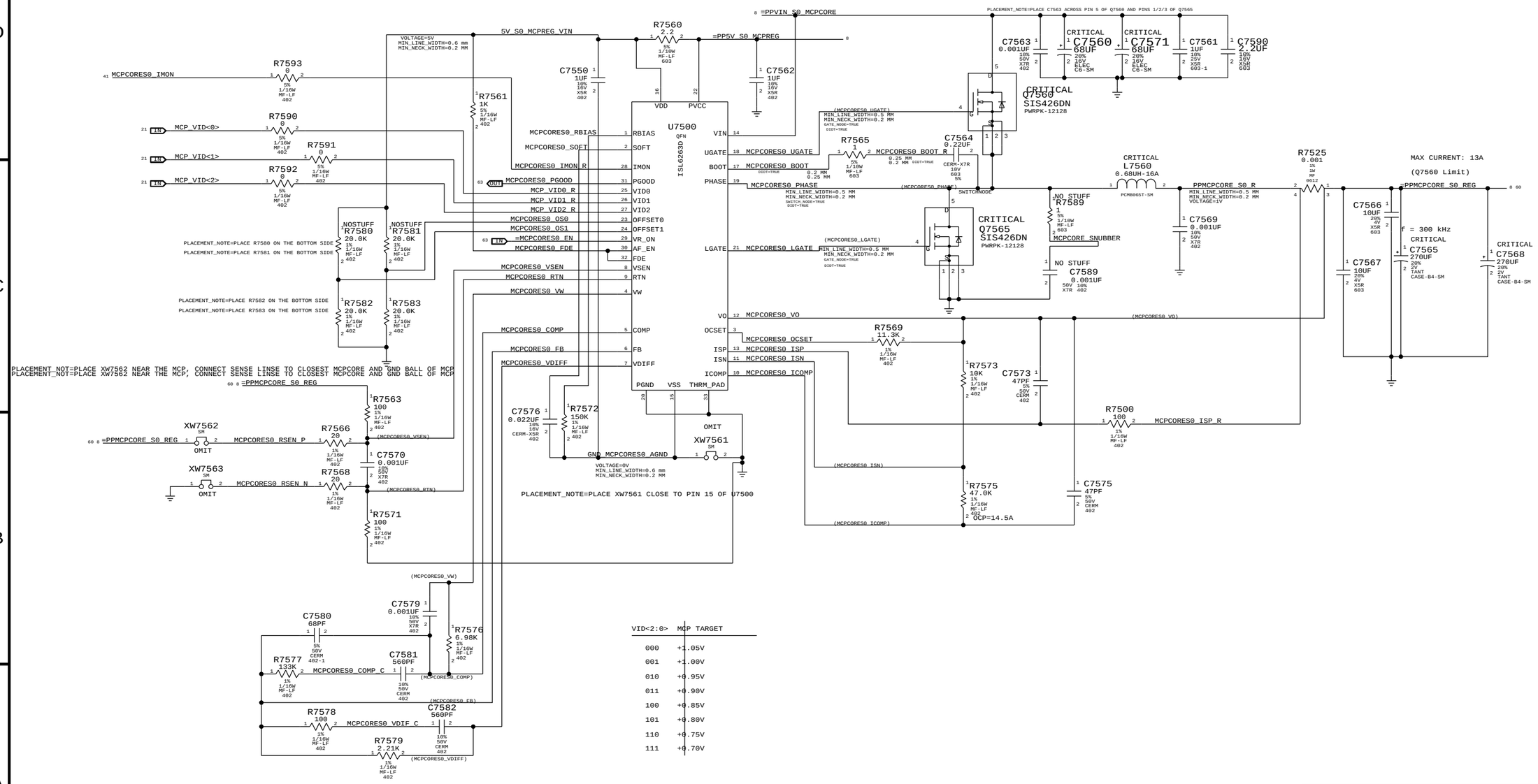

VID<2:0>	MCP TARGET
000	+1.05V
001	+1.00V
010	+0.95V
011	+0.90V
100	+0.85V
101	+0.80V
110	+0.75V
111	+0.70V

SYNC MASTER=K24 MLB SYNC DATE=02/15/2009

PAGE TITLE
MCP CORE REGULATOR

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

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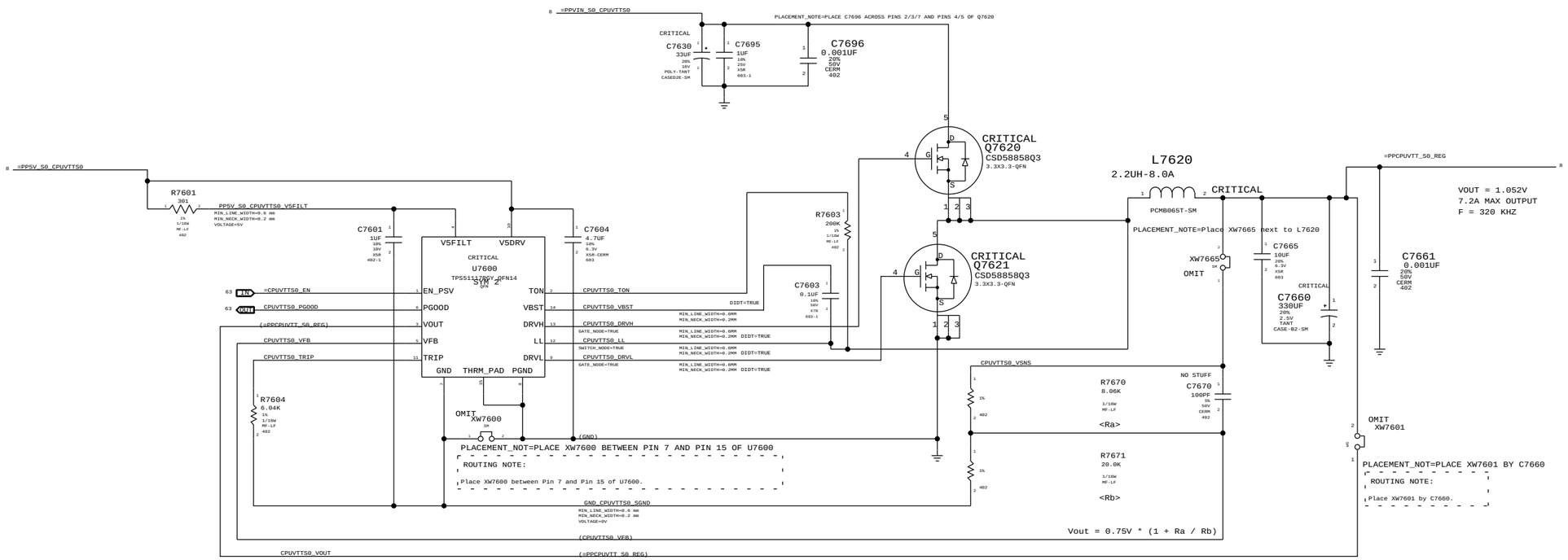
CPUVTT POWER SUPPLY



SYNC MASTER=K24 MLB	SYNC DATE=02/04/2009
PAGE TITLE: CPU VTT(1.05V) SUPPLY	
Apple Inc.	DRAWING NUMBER: 051-7982 — SIZE: D
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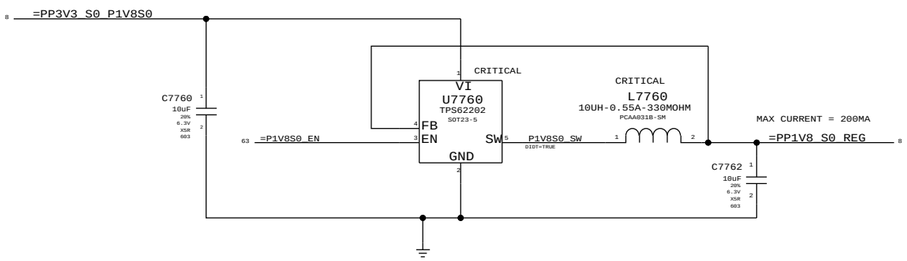
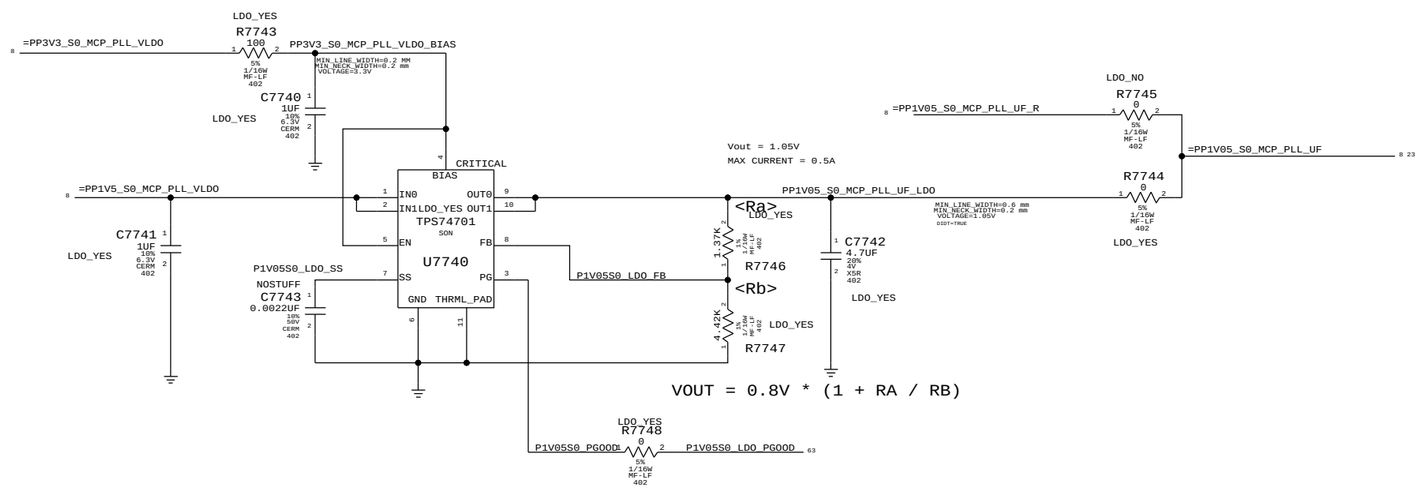
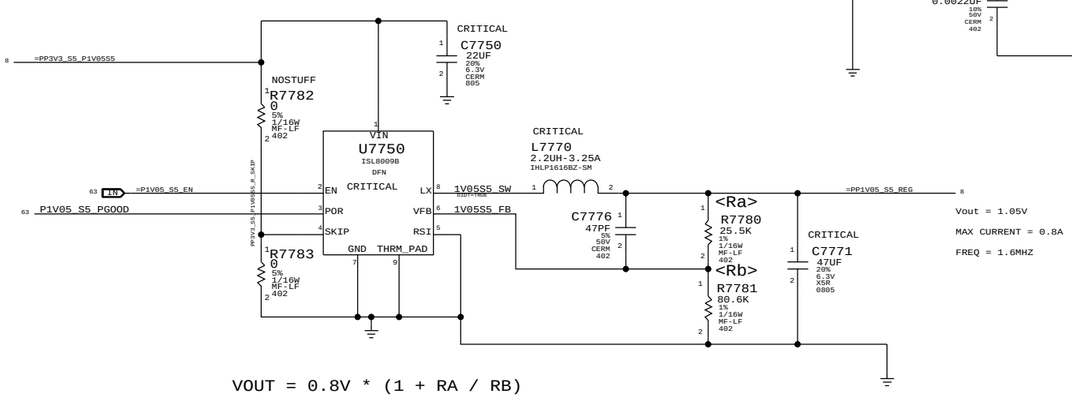
1.8V S0 SWITCHER



1.05V S0 PLL LDO



MCP 1.05V S5 (AUXC) SUPPLY



SYNC MASTER=K24 MLB SYNC DATE=03/24/2009

PAGE TITLE
MISC POWER SUPPLIES

Apple Inc.

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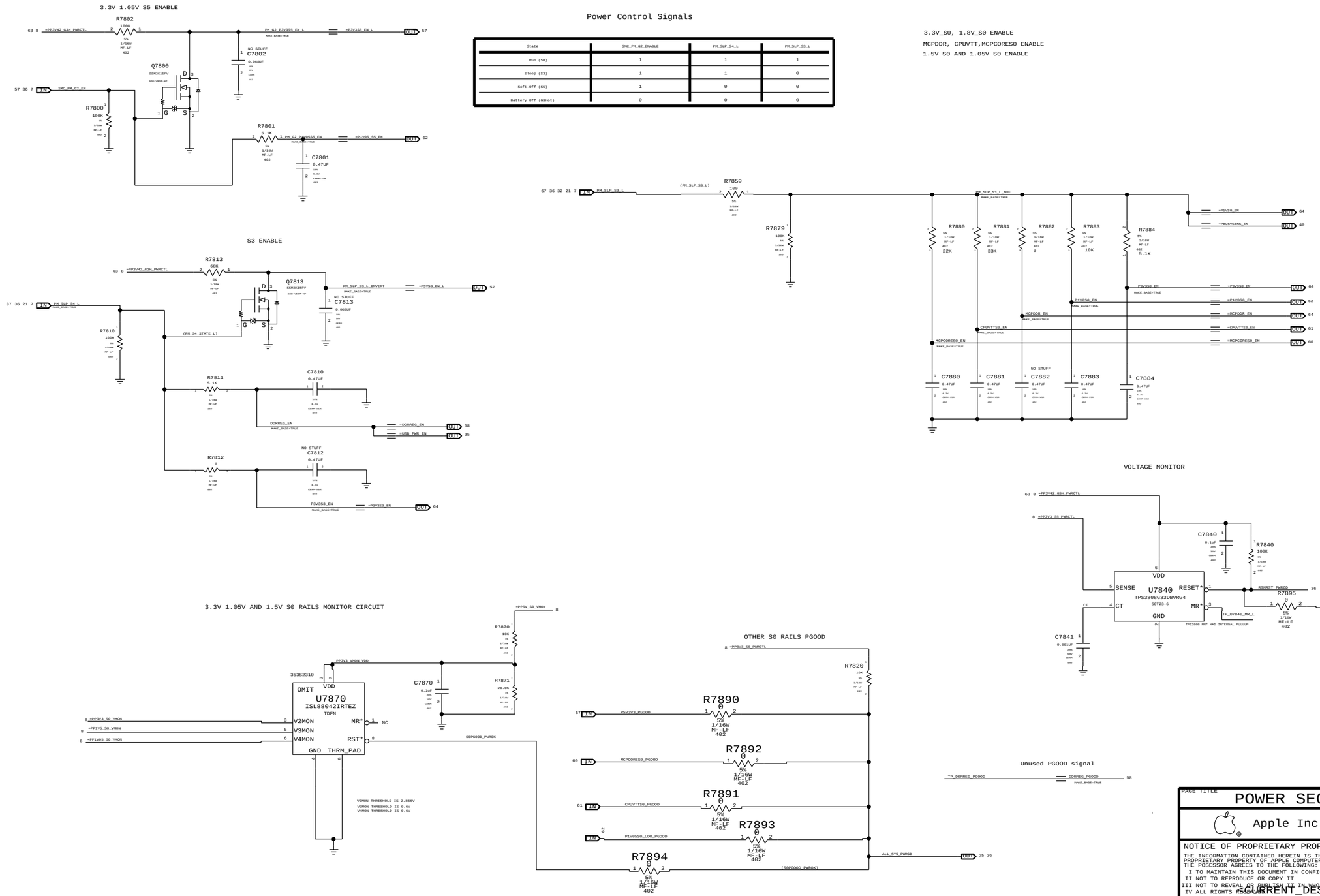

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

PAGE TITLE	
POWER SEQUENCING	
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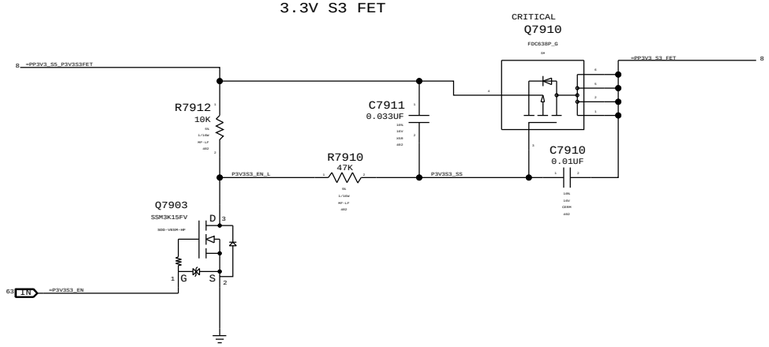
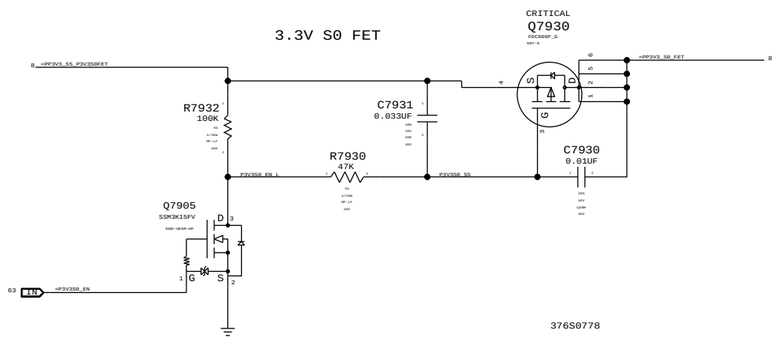
3.3V S3 FET



3.3V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.182 A (EDP)

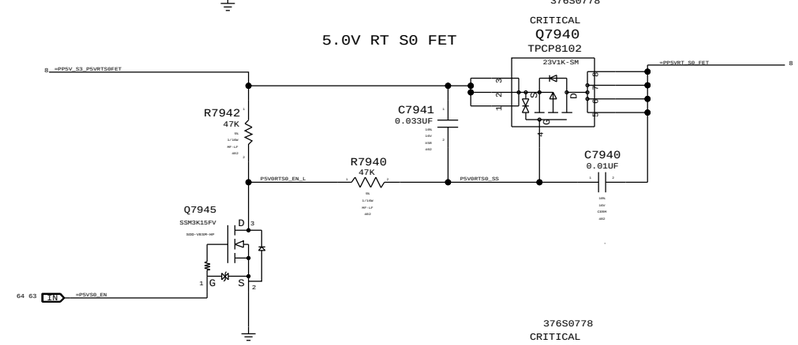
3.3V S0 FET



3.3V S0 FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.431 A (EDP)

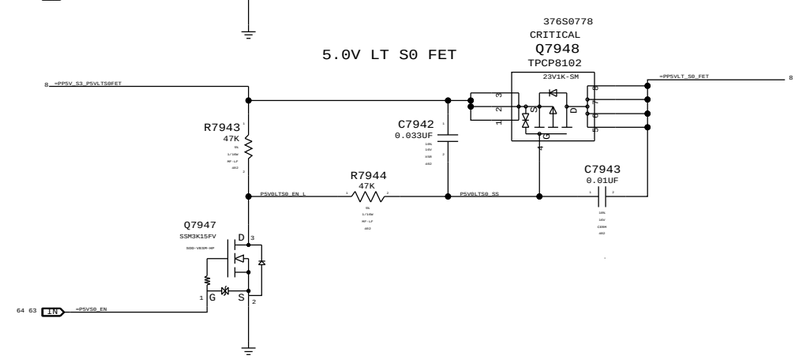
5.0V RT S0 FET



5.0V RT S0 FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	13.5 MOHM @4.5V
LOADING	0.48 A (EDP)

5.0V LT S0 FET

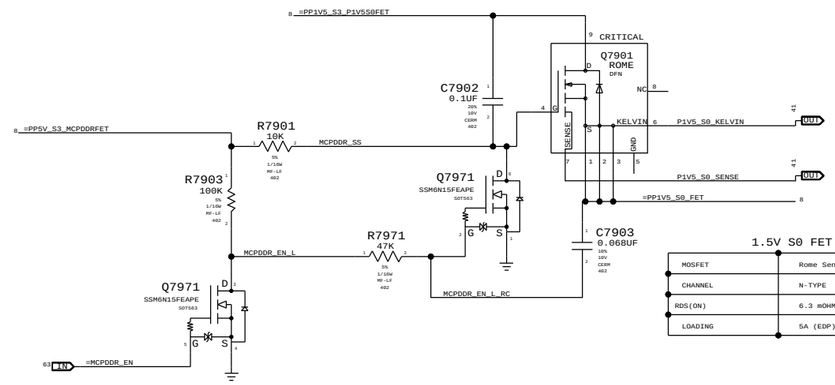


5.0V LT S0 FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	13.5 MOHM @4.5V
LOADING	1.302 A (EDP)

1.5V S0 FET

(1.5V S0 FET FOR DDR3 MEM, MCP79 AND CPU)

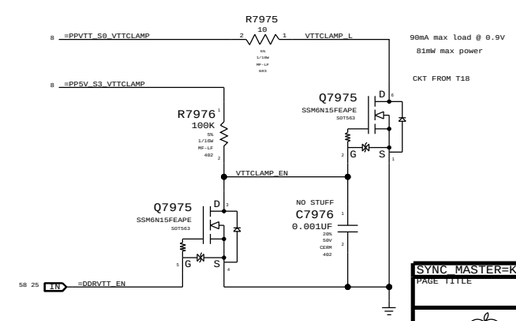


1.5V S0 FET

MOSFET	Rome SenseFET
CHANNEL	N-TYPE
RDS(ON)	6.3 mOHM @4.5V VGS
LOADING	5A (EDP)

MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT
NVIDIA RECOMMENDS UNPOWERING DURING SLEEP.
IN ORDER TO SUPPORT UNPOWERING RAIL, HAREDWARE
MUST GUARANTEE MEM_CKE SIGNALS ARE LOW
BEFORE RAIL IS TURNED OFF, AND REMAINS LOW
UNTIL AFTER RAIL TURNS BACK ON OR DIMMS
WILL EXIT SELF-REFRESH PREMATURELY.
MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP
ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS
LOW THROUGH VTT TERMINATION RESISTORS.



90mA max load @ 0.9V
81mW max power

CKT FROM T18

SYNC_MASTER=K24_MLB SYNC_DATE=02/15/2009

PAGE TITLE
POWER FETS

Apple Inc.

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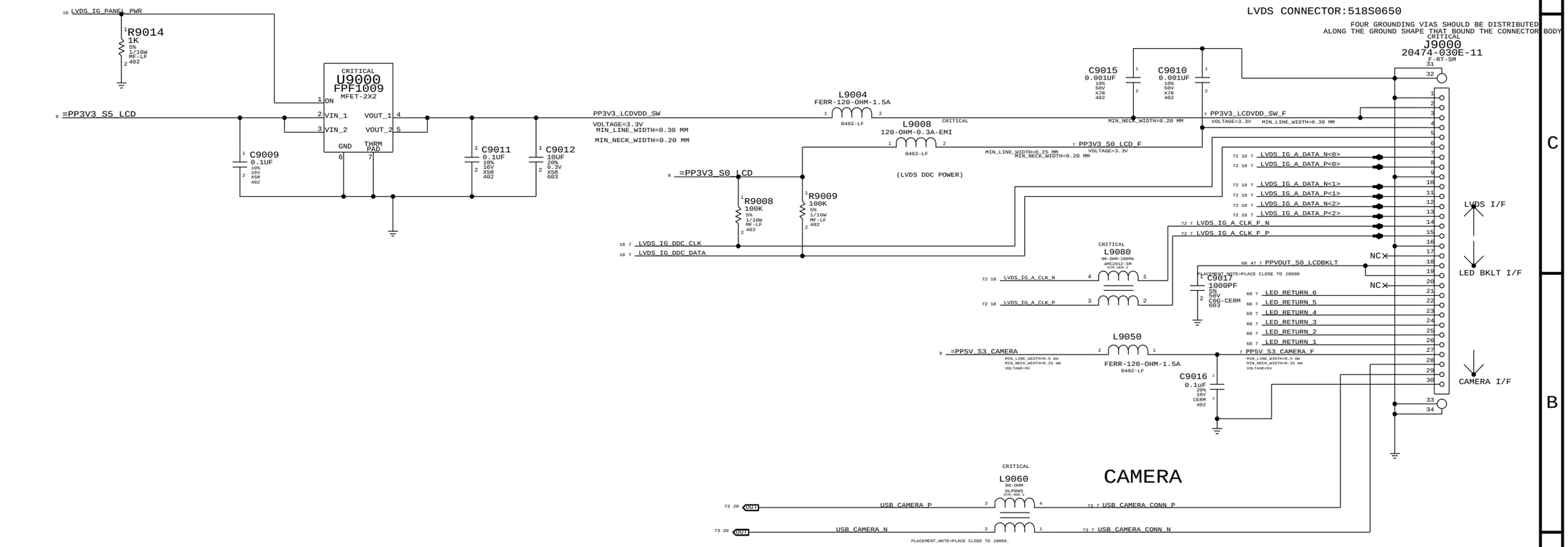
CHECK IF LVDS_IG_PANEL_PWR GLITCHES ON POWER UP



SYNC MASTER=K24 MLB SYNC DATE=02/15/2009

PAGE TITLE
LVDS CONNECTOR

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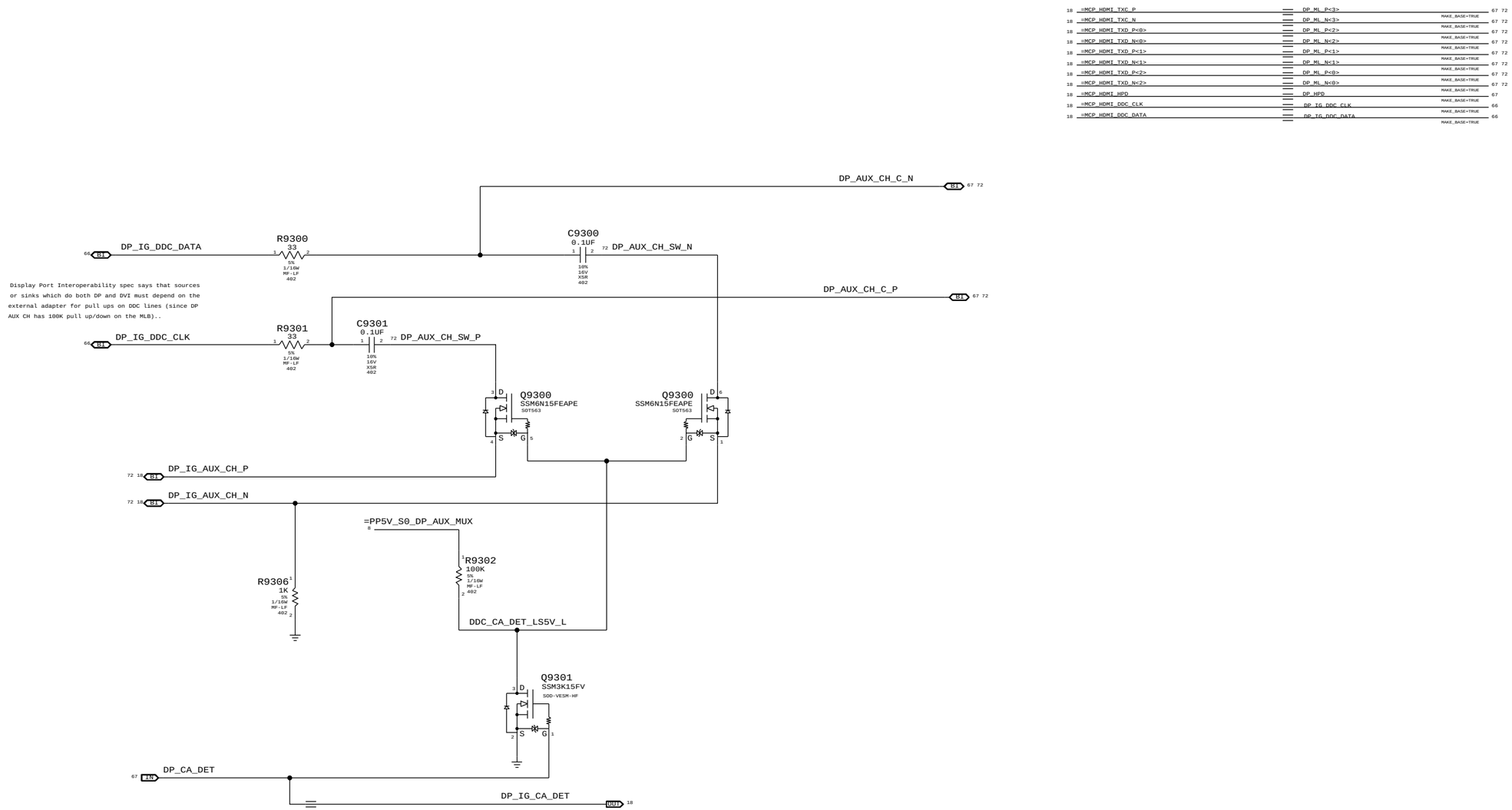

SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

PAGE TITLE
DISPLAYPORT SUPPORT

Apple Inc.

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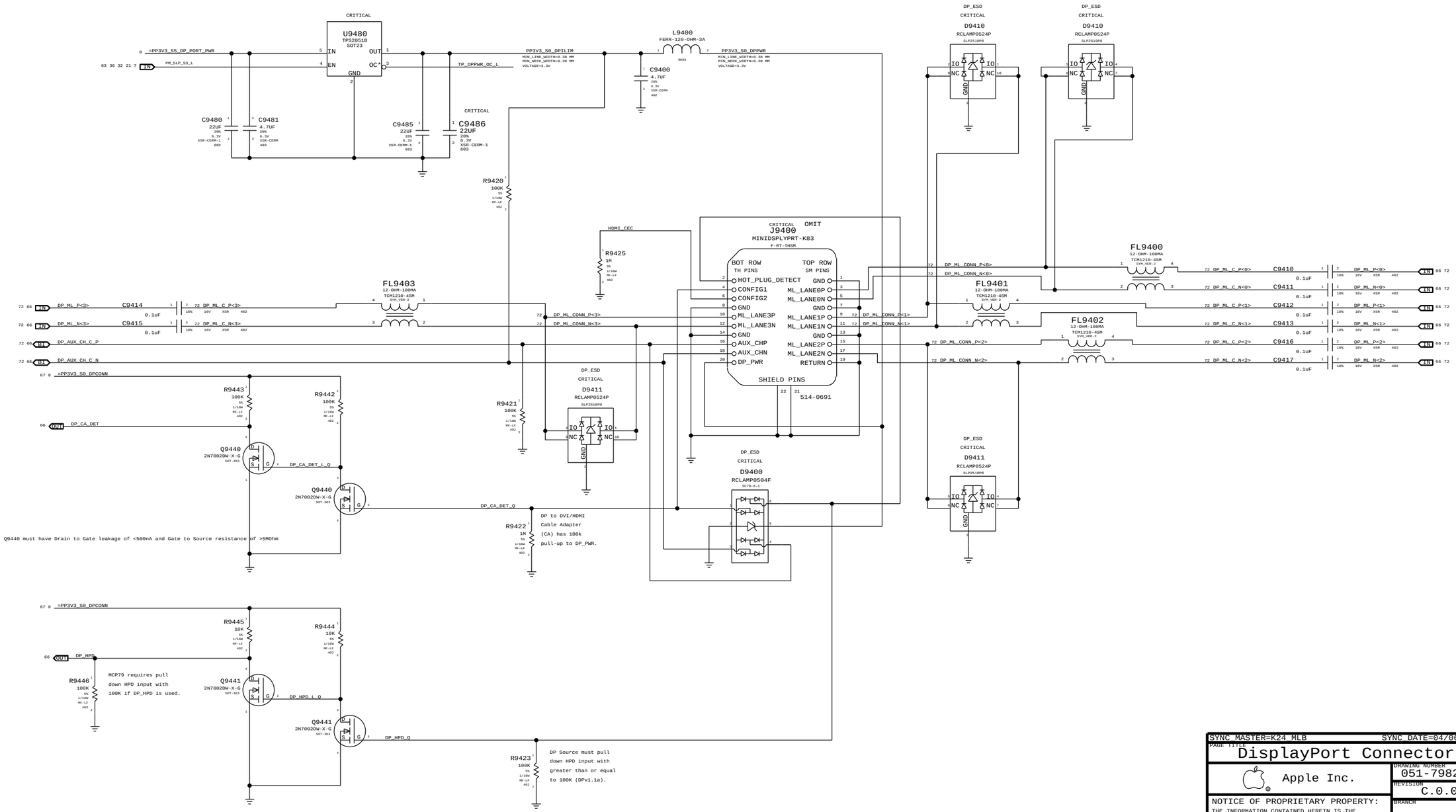
POR IS PLASTIC MINI DP CONNECTOR BUT METAL PART'S SCHEMATIC AND CAD SUMBOLS
HAVE BEEN USED BEACUSE ITS LAND PATTERN CAN ACCOMODATE BOTH TYPES

Port Power Switch



SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

PAGE TITLE
DisplayPort Connector

Apple Inc.

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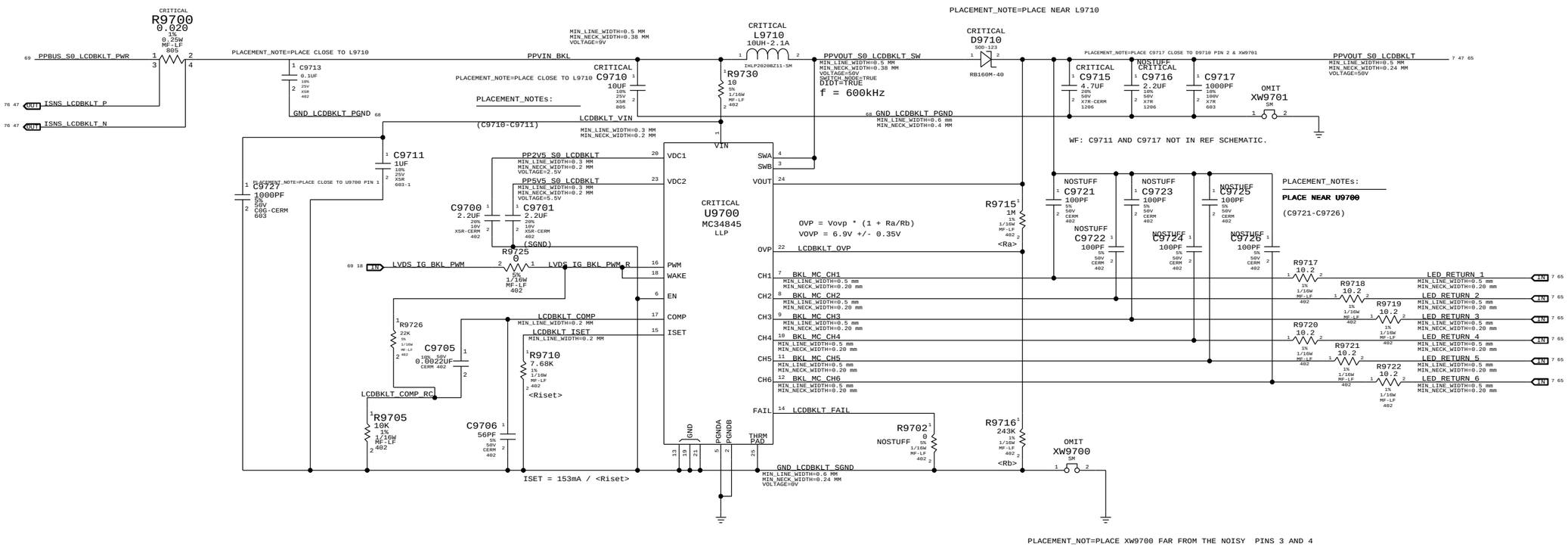

13.3 Inch Panel (9 LEDs per string)

TARGET: ISET = 20MA, OVP = 35V

ACTUAL: ISET = 19.9MA, OVP = 35.2V

SYNC MASTER=VEMURI_K19I SYNC DATE=02/09/2009

PAGE TITLE

LCD Backlight Driver (MC34845)

Apple Inc.

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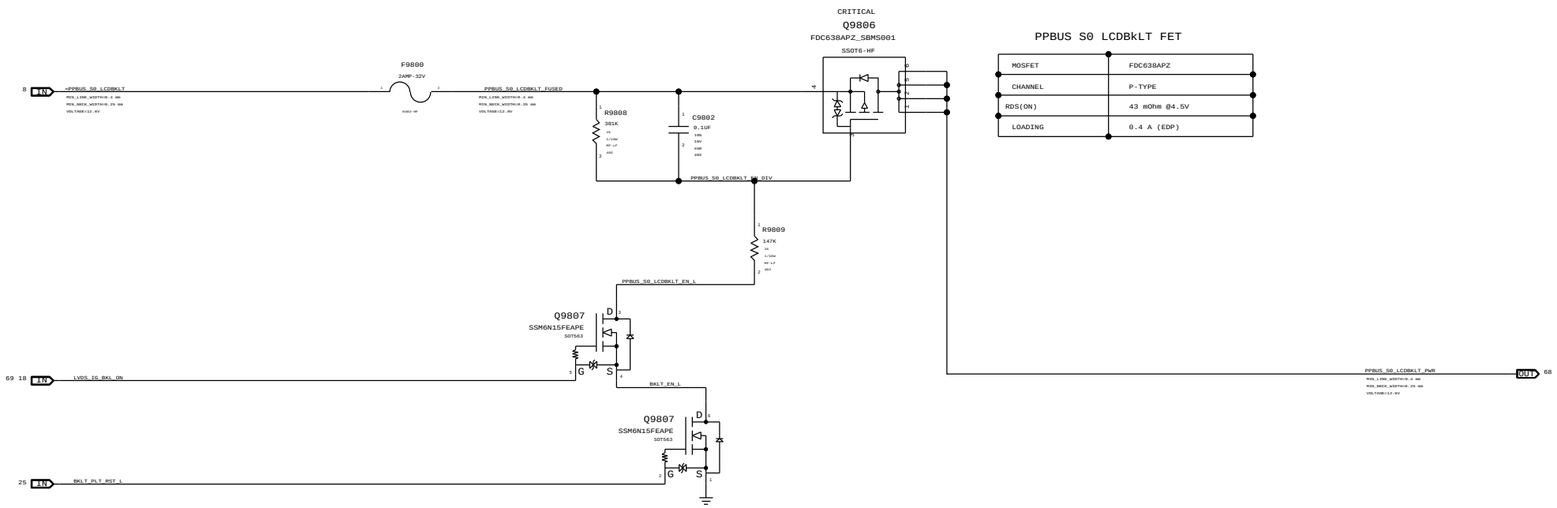
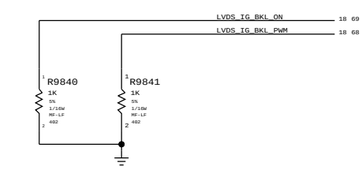


PPBUS S0 LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.4 A (EDP)



MCP HAS INTERNAL 10K PULL-UP FOR THESE SIGNALS

SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

PAGE TITLE
LCD Backlight Support

Apple Inc.

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_BMIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB_4X Signal groups	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_D_L<15..0>	10 14
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_DINV_L<0>	10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0>	10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0>	10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..16>	10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1>	10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1>	10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1>	10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..32>	10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_DINV_L<2>	10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2>	10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2>	10 14
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..48>	10 14
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_DINV_L<3>	10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3>	10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<3>	10 14
FSB_2X Signals	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<16..3>	10 14
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	10 14
	FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	10 14
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..17>	10 14
	FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	10 14
FSB_1X Signals	FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L	10 14
	FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L	10 14
	FSB_BREQ1_L	FSB_50S	FSB_1X	FSB_BREQ1_L	14
	FSB_1X	FSB_50S	FSB_1X	FSB_BNR_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DBSY_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_HIT_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_HITM_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_LOCK_L	10 14
	FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L	10 13 14
	FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0>	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_A20M_L	10 14
	CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	9 10
	CPU_FERR_L	CPU_50S	CPU_BMIL	CPU_FERR_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_IGNNE_L	10 14
	CPU_INIT_L	CPU_50S	CPU_AGTL	CPU_INIT_L	10 14
	CPU_ASYNC_H	CPU_50S	CPU_AGTL	CPU_INTR	10 14
	CPU_ASYNC_H	CPU_50S	CPU_AGTL	CPU_NMI	10 14
	CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 14 37
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 13 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_SMI_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_STPCLK_L	10 14
	PM_THRMTRIP_L	CPU_50S	CPU_BMIL	PM_THRMTRIP_L	10 14 37
	FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L	10 14
	CPU_FROM_SB	CPU_50S	CPU_AGTL	CPU_DPSLP_L	10 14
	CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L	10 14 59
	CPU_ASYNC	CPU_50S	CPU_AGTL	FSB_DPWR_L	10 14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10 14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	13 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	13 14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	14
	CPU_IERR_L	CPU_50S		CPU_IERR_L	10
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	21 59
	(See above)	CPU_50S	CPU_AGTL	IMVP_DPRSLPVR	59
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF	10 26
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10
	XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	10 13
	XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO	10 13
	XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	10 13
	XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	10 13
	XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	10 13
	XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<4..0>	10 13
	XDP_BPM_L5	CPU_50S	CPU_ITP	XDP_BPM_L<5>	10 13
	(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	13
		CPU_50S	CPU_BMIL	CPU_VID<6..0>	11 59
		CPU_50S	CPU_BMIL	IMVP6_VID<6..0>	
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 59
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 59
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	

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CPU/FSB Constraints

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<5..0>	15 27
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<5..0>	15 27
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>	15 27
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CS_L<3..0>	15 27
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_A<14..0>	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_BA<2..0>	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_RAS_L	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_CAS_L	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_WE_L	15 27
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	15 27
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	15 27
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	15 27
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DQ<31..24>	15 27
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	15 27
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DQ<47..40>	15 27
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	15 27
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DQ<63..56>	15 27
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DM<0>	15 27
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DM<1>	15 27
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DM<2>	15 27
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DM<3>	15 27
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DM<4>	15 27
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DM<5>	15 27
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DM<6>	15 27
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DM<7>	15 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	15 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	15 27
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	15 27
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	15 27
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	15 27
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	15 27
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	15 27
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	15 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	15 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	15 27
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<5..0>	15 28
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<5..0>	15 28
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>	15 28
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CS_L<3..0>	15 28
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_A<14..0>	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_BA<2..0>	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_RAS_L	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_CAS_L	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_WE_L	15 28
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	15 28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	15 28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	15 28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	15 28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	15 28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	15 28
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DM<0>	15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DM<1>	15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DM<2>	15 28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DM<3>	15 28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DM<4>	15 28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DM<5>	15 28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DM<6>	15 28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DM<7>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	15 28
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	16
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	16

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v00), Section 2.4

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	v	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v00), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SATA_90D_HDD	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v00), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	30
	PCIE_90D	PCIE	PCIE_MINI_R2D_N	30
PCIE_MINI_R2D	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P	17 30
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N	17 30
PCIE_MINI_D2R	PCIE_90D	PCIE	PCIE_MINI_D2R_P	17 30
	PCIE_90D	PCIE	PCIE_MINI_D2R_N	17 30
	PCIE_90D	PCIE	PCIE_FW_R2D_P	
	PCIE_90D	PCIE	PCIE_FW_R2D_N	
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	9 17
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	9 17
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P	9 17
	PCIE_90D	PCIE	PCIE_FW_D2R_N	9 17
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	17 30
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	17 30
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_P	7 30
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_N	7 30
MCP_PE4_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_P	
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_N	
	PCIE_90D	PCIE	CONN_PCIE_MINI_R2D_P	7 30
	PCIE_90D	PCIE	CONN_PCIE_MINI_R2D_N	7 30
	PCIE_90D	PCIE	CONN_PCIE_MINI_D2R_P	7 30
	PCIE_90D	PCIE	CONN_PCIE_MINI_D2R_N	7 30
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX_CLK_COMP	17
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_P	
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_N	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_P<2..0>	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_N<2..0>	
DP_ML	DP_100D	DISPLAYPORT	DP_ML_P<3..0>	66 67
	DP_100D	DISPLAYPORT	DP_ML_C_P<3..0>	67
DP_ML	DP_100D	DISPLAYPORT	DP_ML_N<3..0>	66 67
	DP_100D	DISPLAYPORT	DP_ML_C_N<3..0>	67
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P	18 66
	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N	18 66
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_P	66
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_N	66
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P	66 67
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N	66 67
MCP_HDMI_RSET	MCP_DV_COMP		MCP_HDMI_RSET	18 24
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP_HDMI_VPROBE	18 24
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	18 65
	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_P	7 65
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	18 65
	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_N	7 65
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>	7 18 65
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>	7 18 65
DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0>	67
	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0>	67
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET	18 24
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE	18 24
SATA_HDD_R2D	SATA_90D_HDD	SATA	SATA_HDD_R2D_C_P	20 34
	SATA_90D_HDD	SATA	SATA_HDD_R2D_C_N	20 34
	SATA_90D_HDD	SATA	SATA_HDD_R2D_P	7 34
	SATA_90D_HDD	SATA	SATA_HDD_R2D_N	7 34
	SATA_90D_HDD	SATA	SATA_HDD_R2D_UF_P	34
	SATA_90D_HDD	SATA	SATA_HDD_R2D_UF_N	34
SATA_HDD_D2R	SATA_90D_HDD	SATA	SATA_HDD_D2R_P	20 34
	SATA_90D_HDD	SATA	SATA_HDD_D2R_N	20 34
	SATA_90D_HDD	SATA	SATA_HDD_D2R_C_P	7 34
	SATA_90D_HDD	SATA	SATA_HDD_D2R_C_N	7 34
	SATA_90D_HDD	SATA	SATA_HDD_D2R_UF_P	34
	SATA_90D_HDD	SATA	SATA_HDD_D2R_UF_N	34
SATA_ODD_R2D	SATA_100D	SATA	SATA_ODD_R2D_C_P	20 34
	SATA_100D	SATA	SATA_ODD_R2D_C_N	20 34
	SATA_100D	SATA	SATA_ODD_R2D_P	7 34
	SATA_100D	SATA	SATA_ODD_R2D_N	7 34
	SATA_100D	SATA	SATA_ODD_R2D_UF_P	34
	SATA_100D	SATA	SATA_ODD_R2D_UF_N	34
SATA_ODD_D2R	SATA_100D	SATA	SATA_ODD_D2R_P	20 34
	SATA_100D	SATA	SATA_ODD_D2R_N	20 34
	SATA_100D	SATA	SATA_ODD_D2R_C_P	7 34
	SATA_100D	SATA	SATA_ODD_D2R_C_N	7 34
	SATA_100D	SATA	SATA_ODD_D2R_UF_P	34
	SATA_100D	SATA	SATA_ODD_D2R_UF_N	34
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP	20

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7,.0>	13 19
PCI_AD	PCI_55S	PCI	PCI_AD<23,.8>	
PCI_AD24	PCI_55S	PCI	PCI_AD<24>	
PCI_AD	PCI_55S	PCI	PCI_AD<31,.25>	
PCI_AD	PCI_55S	PCI	PCI_PAR	
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3,.0>	
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L	
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L	
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L	
PCI_REQ0_L	PCI_55S	PCI	PCI_REQ0_L	19
PCI_GNT0_L	PCI_55S	PCI	PCI_GNT0_L	
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	19
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L	
PCI_INTW_L	PCI_55S	PCI	PCI_INTW_L	
PCI_INTX_L	PCI_55S	PCI	PCI_INTX_L	
PCI_INTY_L	PCI_55S	PCI	PCI_INTY_L	
PCI_INTZ_L	PCI_55S	PCI	PCI_INTZ_L	
MCP_PCI_CLK2	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R	19
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP	19
LPC_AD	LPC_55S	LPC	LPC_AD<3,.0>	19 36 38
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L	19 36 38
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L	19 25
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	19 25
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	25 36
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	25 38
USB_EXTA	USB_90D	USB	USB_EXTA_P	20 35
	USB_90D	USB	USB_EXTA_N	20 35
	USB_90D	USB	USB_EXTA_MUXED_P	35
	USB_90D	USB	USB_EXTA_MUXED_N	35
	USB_90D	USB	CONN_USB_EXTA_P	35
	USB_90D	USB	CONN_USB_EXTA_N	35
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	20 65
	USB_90D	USB	USB_CAMERA_N	20 65
	USB_90D	USB	USB_CAMERA_CONN_P	7 65
	USB_90D	USB	USB_CAMERA_CONN_N	7 65
USB_BT	USB_90D	USB	USB_BT_P	20 30
	USB_90D	USB	USB_BT_N	20 30
	USB_90D	USB	CONN_USB2_BT_P	7 30
	USB_90D	USB	CONN_USB2_BT_N	7 30
USB_TPAD	USB_90D	USB	USB_TPAD_P	20 44
	USB_90D	USB	USB_TPAD_N	20 44
	USB_90D	USB	USB_TPAD_R_P	44
	USB_90D	USB	USB_TPAD_R_N	44
USB_IR	USB_90D	USB	USB_IR_P	9 20
	USB_90D	USB	USB_IR_N	9 20
USB_EXTB	USB_90D	USB	USB_EXTB_P	20 35
	USB_90D	USB	USB_EXTB_N	20 35
	USB_90D	USB	CONN_USB_EXTB_P	35
	USB_90D	USB	CONN_USB_EXTB_N	35
USB_SD	USB_90D	USB	USB_CARDREADER_P	9 20
	USB_90D	USB	USB_CARDREADER_N	9 20
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND	20
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK	13 21 39
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA	13 21 39
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK	21 39
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA	21 39
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	21 49
	HDA_55S	HDA	HDA_BIT_CLK_R	21
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	21 49
	HDA_55S	HDA	HDA_SYNC_R	21
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L	21
	HDA_55S	HDA	HDA_RST_L	21 49
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	21 49
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	21 49
	HDA_55S	HDA	HDA_SDOUT_R	21
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP	21
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R	21 25
	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	25 36
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	21 38 48
	SPI_55S	SPI	SPI_CLK	48
	SPI_55S	SPI	SPI_ALT_CLK	38
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	21 38 48
	SPI_55S	SPI	SPI_MOSI	48
	SPI_55S	SPI	SPI_ALT_MOSI	38
SPI_MISO	SPI_55S	SPI	SPI_MISO	21 38 48
	SPI_55S	SPI	SPI_MISO_R	48
	SPI_55S	SPI	SPI_ALT_MISO	38
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	21 38
	SPI_55S	SPI	SPI_CS0_L	
	SPI_55S	SPI	SPI_CS1_R_L	
	SPI_55S	SPI	SPI_CS1_R_L_USE_MLB	

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	18
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	18
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	18 32
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	31 32
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	18 31
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	18 31
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	31
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	18 31
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>	31
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD<0>	18 31
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	18 31
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	18 31
	ENET_MII_55S	ENET_MII	ENET_RXCTL_R	31
	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK_R	31
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	18 31
ENET_TXD0	ENET_MII_55S	ENET_MII	ENET_TXD<0>	18 31
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	18 31
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	18 31
	ENET_MII_55S	ENET_MII	ENET_RESET_L	18 31
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	31 33
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	31 33
	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_P<3..0>	33
	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_N<3..0>	33

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_A_S3_SCL	SMB_555	SMB	SMBUS_SMC_A_S3_SCL	7 39
SMBUS_SMC_A_S3_SDA	SMB_555	SMB	SMBUS_SMC_A_S3_SDA	7 39
SMBUS_SMC_B_S0_SCL	SMB_555	SMB	SMBUS_SMC_B_S0_SCL	39
SMBUS_SMC_B_S0_SDA	SMB_555	SMB	SMBUS_SMC_B_S0_SDA	39
SMBUS_SMC_0_S0_SCL	SMB_555	SMB	SMBUS_SMC_0_S0_SCL	39
SMBUS_SMC_0_S0_SDA	SMB_555	SMB	SMBUS_SMC_0_S0_SDA	39
SMBUS_SMC_BSA_SCL	SMB_555	SMB	SMBUS_SMC_BSA_SCL	7 39
SMBUS_SMC_BSA_SDA	SMB_555	SMB	SMBUS_SMC_BSA_SDA	7 39
SMBUS_SMC_MGMT_SCL	SMB_555	SMB	SMBUS_SMC_MGMT_SCL	39
SMBUS_SMC_MGMT_SDA	SMB_555	SMB	SMBUS_SMC_MGMT_SDA	39

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P
	1TO1_DIFFPAIR		CHGR_CSI_N
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P
	1TO1_DIFFPAIR		CHGR_CSO_N

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SMC Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

K84 SENSOR NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DIFFPAIR		CHGR_CSO_R_P	56
	DIFFPAIR		CHGR_CSO_R_N	56
	DIFFPAIR		CPUTHMSNS_D2_P	42
	DIFFPAIR		CPUTHMSNS_D2_N	42
	DIFFPAIR		CPU_THERMD_P	10 42
	DIFFPAIR		CPU_THERMD_N	10 42
	DIFFPAIR		ISNS_CPUVTT_P	41
	DIFFPAIR		ISNS_CPUVTT_N	41
	DIFFPAIR		ISNS_HDD_P	34 47
	DIFFPAIR		ISNS_HDD_N	34 47
	DIFFPAIR		ISNS_HDD_R_P	47
	DIFFPAIR		ISNS_HDD_R_N	47
	DIFFPAIR		MCPTHMSNS_D2_P	42
	DIFFPAIR		MCPTHMSNS_D2_N	42
	DIFFPAIR		MCP_THMDIODE_P	21 42
	DIFFPAIR		MCP_THMDIODE_N	21 42
	DIFFPAIR		ISNS_ODD_P	34 47
	DIFFPAIR		ISNS_ODD_N	34 47
	DIFFPAIR		ISNS_ODD_R_P	47
	DIFFPAIR		ISNS_ODD_R_N	47
	DIFFPAIR		ISNS_AIRPORT_P	30 47
	DIFFPAIR		ISNS_AIRPORT_N	30 47
	DIFFPAIR		ISNS_AIRPORT_R_P	47
	DIFFPAIR		ISNS_AIRPORT_R_N	47
	DIFFPAIR		ISNS_1V5_S3_P	47 58
	DIFFPAIR		ISNS_1V5_S3_N	47 58
	DIFFPAIR		ISNS_1V5_S3_R_P	47
	DIFFPAIR		ISNS_1V5_S3_R_N	47
	DIFFPAIR		ISNS_LCDBKLT_P	47 68
	DIFFPAIR		ISNS_LCDBKLT_N	47 68

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K84 SPECIAL CONSTRAINTS

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K84 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	0.100MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.115 MM	0.115 MM			
50_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.100 MM			
40_OHM_SE	*	Y	0.126 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	*	Y	0.222 MM	0.222 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.151 MM	0.100 MM	=STANDARD	0.224 MM	0.224 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.100 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF_HDD	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF_HDD	ISL3,ISL4,ISL9,ISL10	Y	0.083 MM	0.083 MM		0.400 MM	0.400 MM
100_OHM_DIFF_HDD	TOP,BOTTOM	Y	0.095 MM	0.095 MM		0.400 MM	0.400 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	TOP,BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.350 MM	?
2X_DIELECTRIC	-	0.126 MM	?
3X_DIELECTRIC	-	0.189 MM	?
4X_DIELECTRIC	-	0.252 MM	?
5X_DIELECTRIC	-	0.315 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_LPC	*	BGA_P1MM	BGA_P2MM
CLK_PCI	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P2MM
CLK_SLOW	*	BGA_P1MM	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P3MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA_P1MM	STANDARD
MEM_40S_VDD	BGA_P1MM	STANDARD

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K84 RULE DEFINITIONS

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